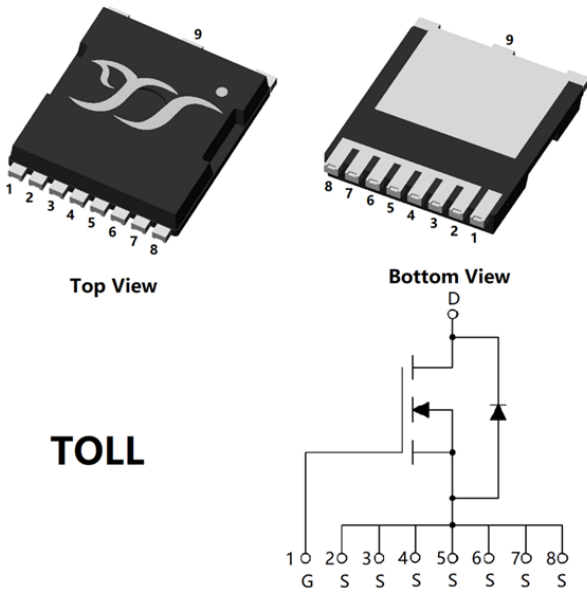


N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 100V
- I_D 265A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<2.1m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Load switch
- Battery management
- Solar

■ Absolute Maximum Ratings ($T_J=25^\circ C$ unless otherwise noted)

Parameter			Symbol	Limit	Unit
Drain-source Voltage			V_{DS}	100	V
Gate-source Voltage			V_{GS}	± 20	V
Continuous Drain Current (Note 1,2)	Steady-State	$T_A=25^\circ C$	I_D	25	A
		$T_A=100^\circ C$		17	
Continuous Drain Current (Note 1,3)	Steady-State	$T_C=25^\circ C$		265	
		$T_C=100^\circ C$		187	
Pulsed Drain Current	$T_C=25^\circ C, t_p=100\mu s$		I_{DM}	1060	A
Avalanche energy	$V_G=10V, R_G=25\Omega, L=2mH, I_{AS}=38.5A$		EAS	1482	mJ
Total Power Dissipation (Note 1,2)	Steady-State	$T_A=25^\circ C$	P_D	3.3	W
		$T_A=100^\circ C$		1.6	
Total Power Dissipation (Note 1,3)	Steady-State	$T_C=25^\circ C$		375	
		$T_C=100^\circ C$		187	
Junction and Storage Temperature Range			T_J, T_{STG}	-55~+175	$^\circ C$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	35	45	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.3	0.4	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJT2D1G10H	F1	YJT2D1G10H	2000	4000	20000	13" reel



YJT2D1G10H

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	100	-	-	V
		V _{GS} = 0V, I _D =1mA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
		V _{DS} =100V, V _{GS} =0V, T _J =125°C	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	2.2	3.0	3.8	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =50A	-	1.5	2.1	mΩ
Diode Forward Voltage	V _{SD}	I _S =30A, V _{GS} =0V	-	-	1.2	V
Gate resistance	R _G	f=1MHz	-	0.85	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	265	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHz	-	9600	-	pF
Output Capacitance	C _{oss}		-	3245	-	
Reverse Transfer Capacitance	C _{rss}		-	48	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =50A	-	132.5	-	nC
Gate-Source Charge	Q _{gs}		-	55	-	
Gate-Drain Charge	Q _{gd}		-	17	-	
Reverse Recovery Charge	Q _{rr}	I _F =50A, di/dt=100A/us	-	157	-	nC
Reverse Recovery Time	t _{rr}		-	93	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _D =50A R _{GEN} =3Ω	-	30	-	ns
Turn-on Rise Time	t _r		-	48	-	
Turn-off Delay Time	t _{D(off)}		-	59	-	
Turn-off fall Time	t _f		-	34	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of R_{θJA} is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with T_A =25°C. The maximum allowed junction temperature of 175°C. The value in any given application depends on the user's specific board design.
- Thermal resistance from junction to soldering point (on the exposed drain pad).



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Typical Electrical and Thermal Characteristics Diagrams

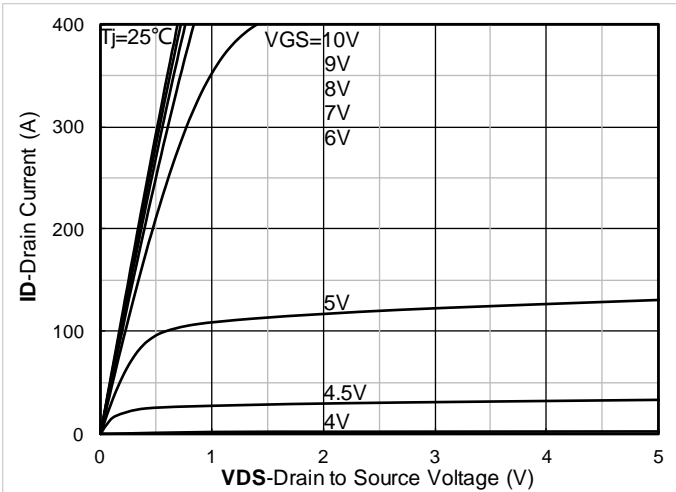


Figure 1. Output Characteristics

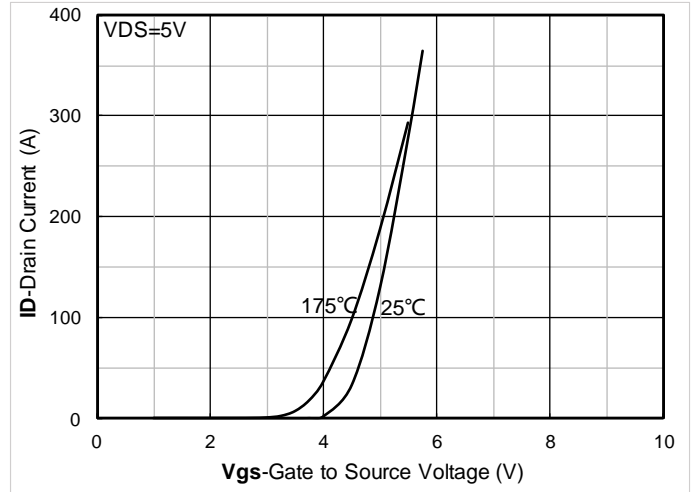


Figure 2. Transfer Characteristics

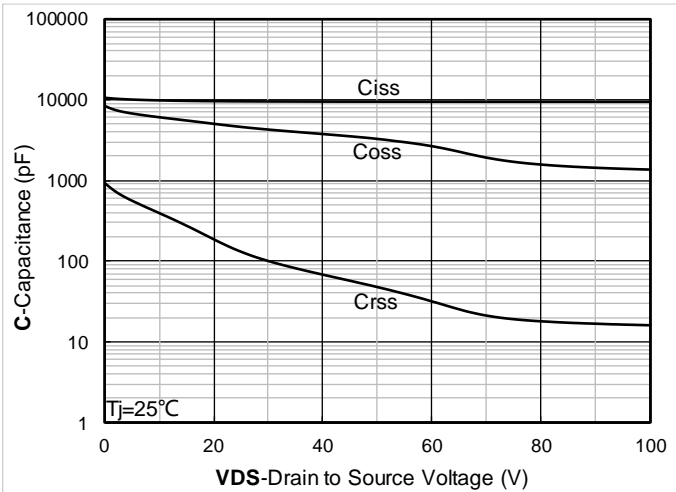


Figure 3. Capacitance Characteristics

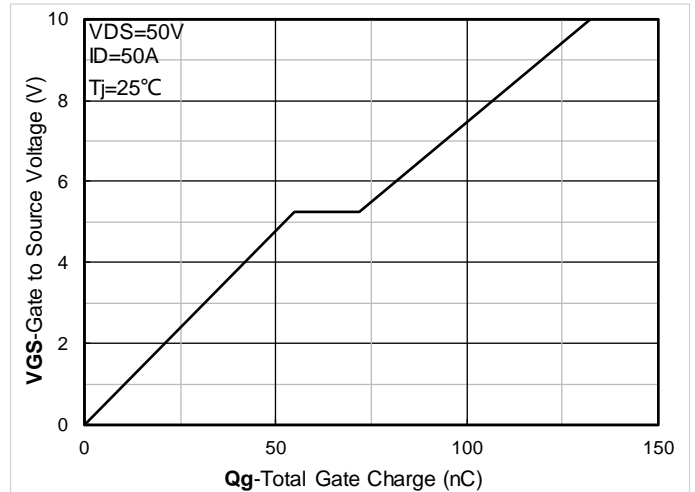


Figure 4. Gate Charge

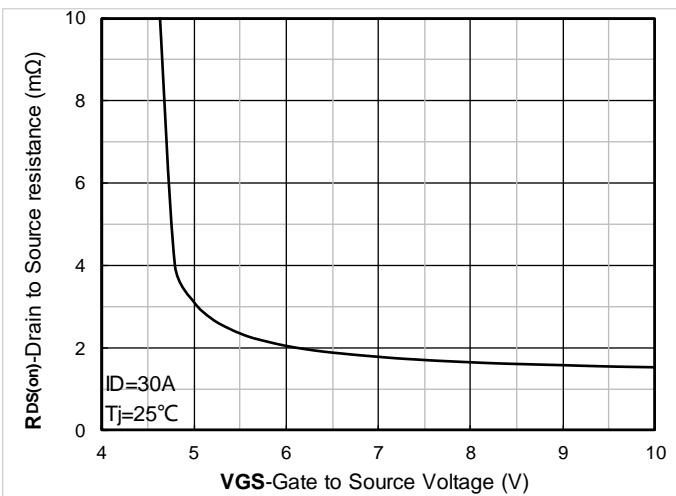


Figure 5. On-Resistance vs Gate to Source Voltage

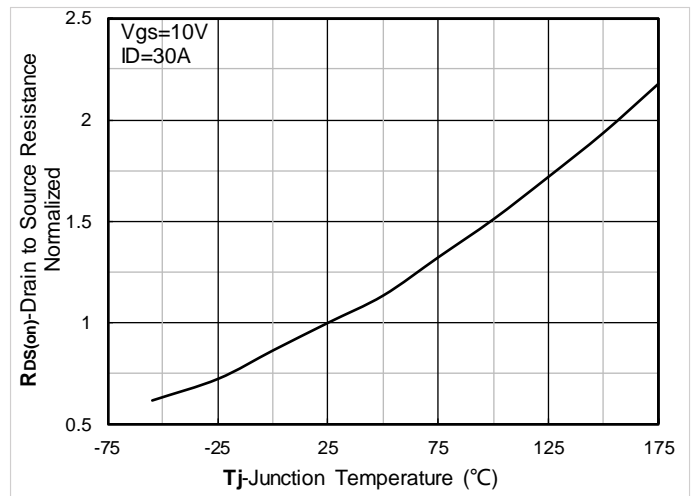


Figure 6. Normalized On-Resistance



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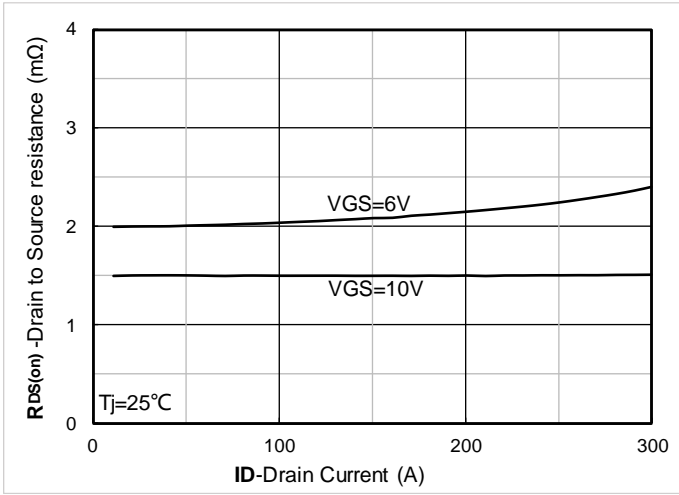


Figure 7. $R_{DS(on)}$ VS Drain Current

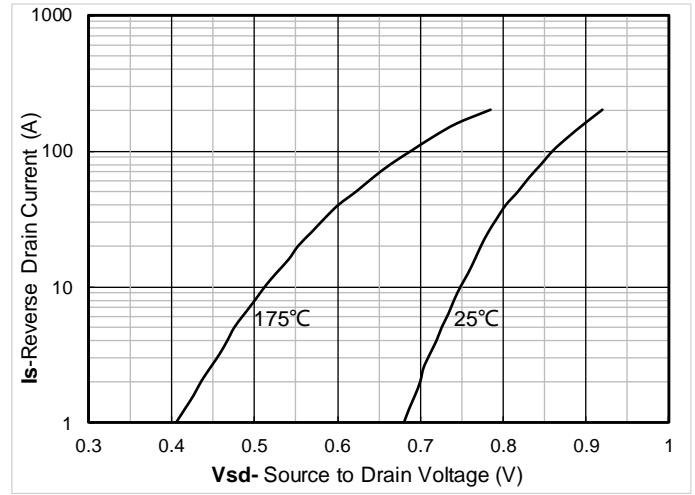


Figure 8. Forward characteristics of reverse diode

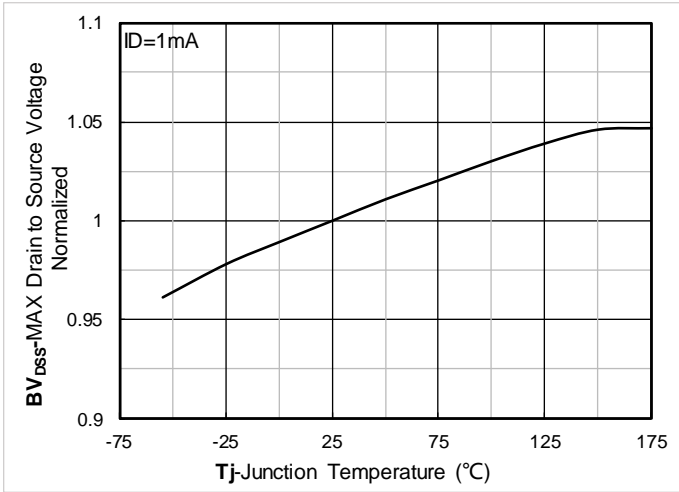


Figure 9. Normalized breakdown voltage

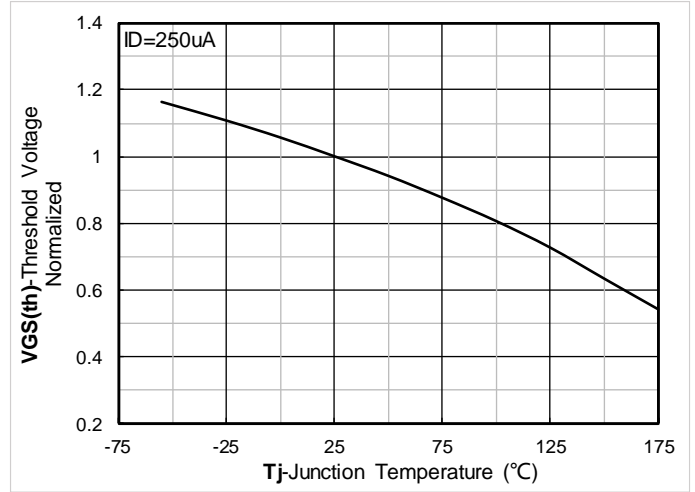


Figure 10. Normalized Threshold voltage

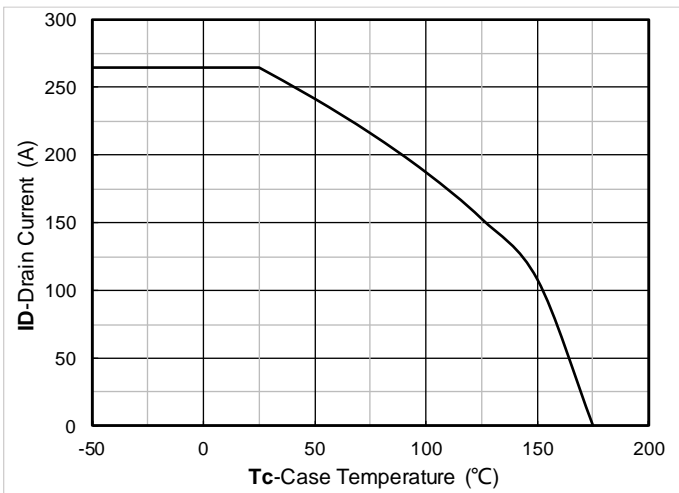


Figure 11. Current dissipation

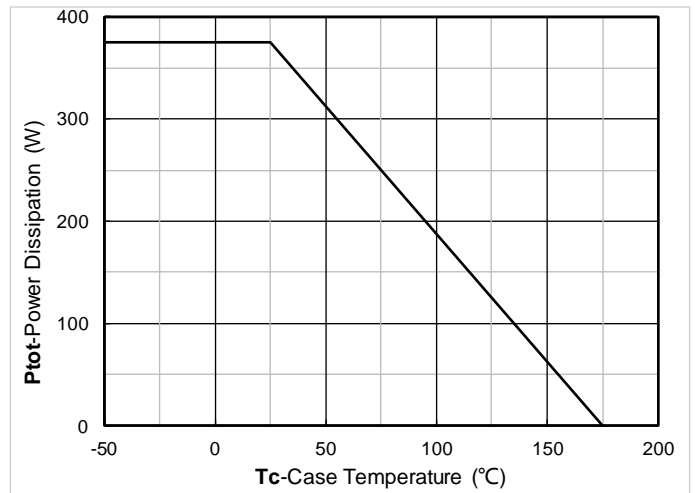


Figure 12. Power dissipation

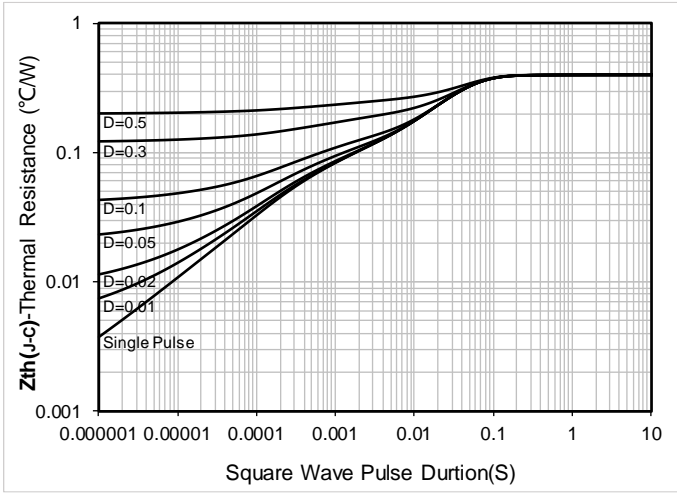


Figure 13. Maximum Transient Thermal Impedance

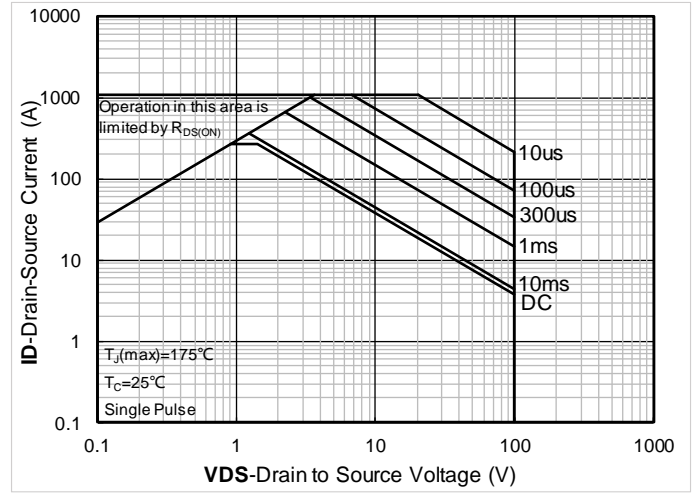


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

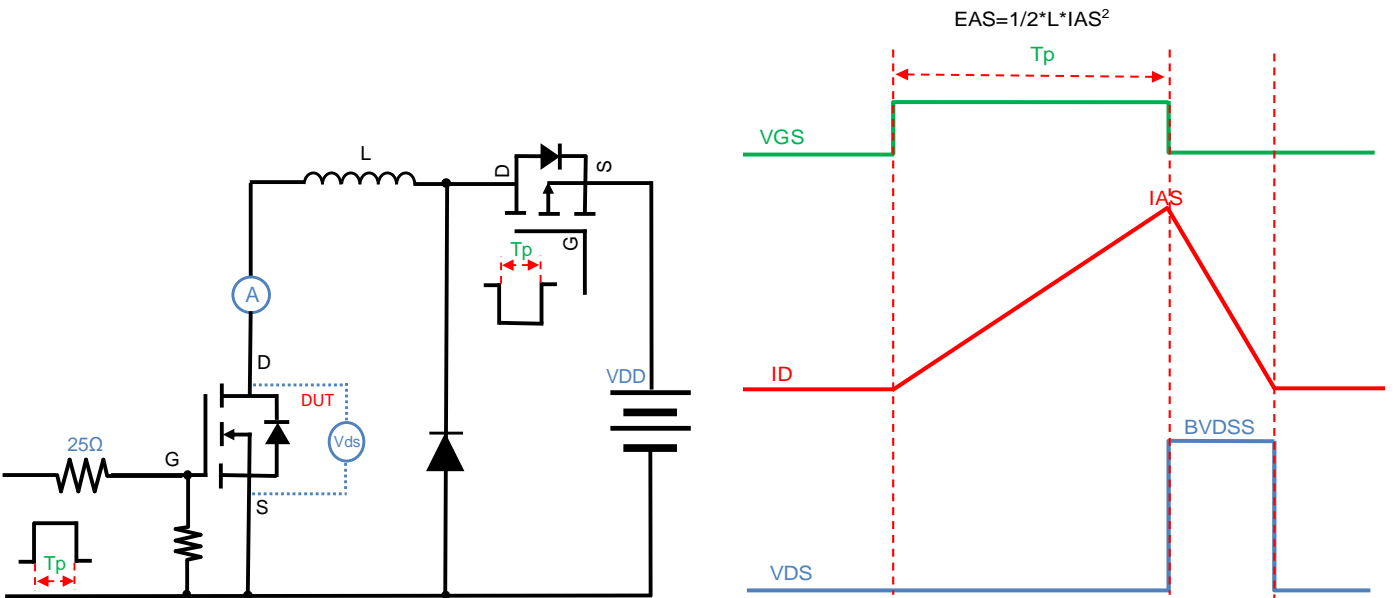


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

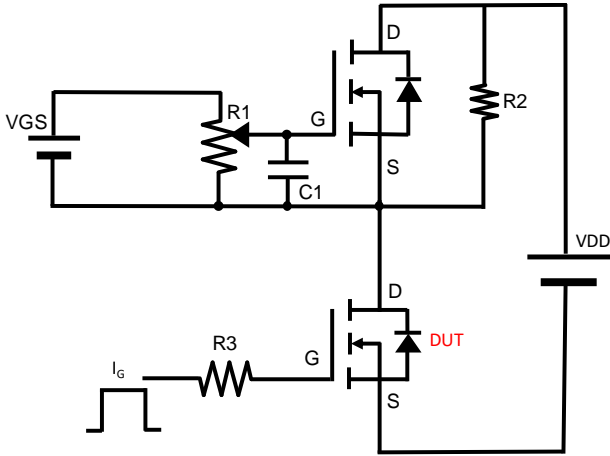


Figure B. Gate Charge Test Circuit & Waveform

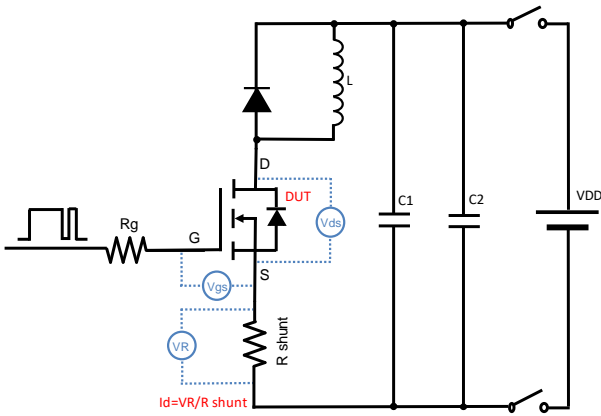


Figure C. Resistive Switching Test Circuit & Waveform

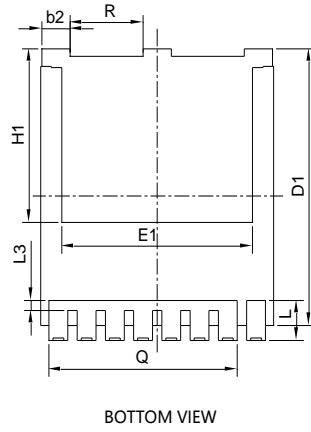
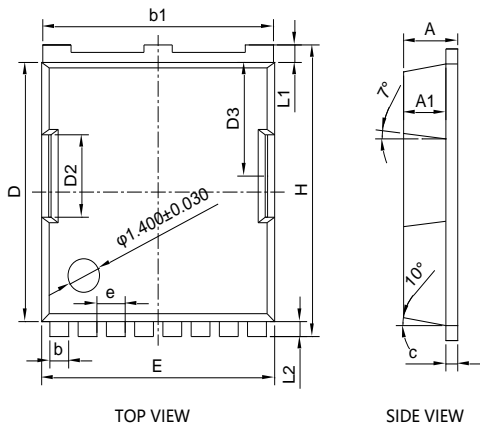


Figure D. Diode Recovery Test Circuit & Waveform

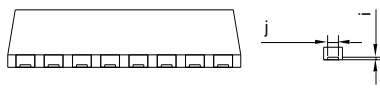


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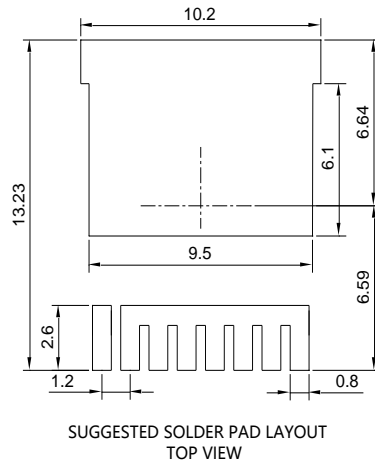
■ TOLL Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.2	2.3	2.4
A1	1.7	1.8	1.9
b	0.7	0.8	0.9
b1	9.7	9.8	9.9
b2	1.1	1.2	1.3
c	0.4	0.5	0.6
D	10.28	10.38	10.48
D1	10.98	11.08	11.18
D2	3.2	3.3	3.4
D3	4.45	4.55	4.65
E	9.8	9.9	10
E1	8	8.1	8.2
e	1.2 BSC		
H	11.58	11.68	11.78
H1	6.95 BSC		
i	0.1 REF		
j	0.46 REF		
L	1.5	1.6	1.7
L1	0.6	0.7	0.8
L2	0.5	0.6	0.7
L3	0.3	0.4	0.5
Q	8 REF		
R	3.0	3.1	3.2



- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.03\text{mm}$.
 3. The pad layout is for reference purposes only.



UNIT: mm



YJT2D1G10H

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