Lead-free Green

6V / 500mA Low Drop-out Linear Regulator

Description

JLR501 is a low drop-out linear regulator offering high output current of 500mA at fixed output voltages. While the drop-out voltage is as low as 130mV over I_{OUT} = 100mA, the quiescent current measured is an ultra-low 0.8μA typically.

PSRR performance of 65dB @ 1kHz and noise performance at 70μV_{RMS} make the device a good fit for applications (e.g. 4G, WiFi module) in which clean supply power line is often deemed essential. As a result, signal integrity and reliable operation of sensitive analog circuitry powered can be assured. Armed with comprehensive protection features (thermal shut-down, short-circuit, current limiting) and precision band-gap reference, the device delivers accurate (± 2%) output voltages at the following fixed levels: 1.8V, 2.8V, 3.3V.

JLR501 is manufactured [halogen, lead, antimony] free and RoHS compliant. Packages offered: DFN1010-4L, SOT-23-5L, SOT89-3L.

Features and Benefits

- High accuracy (tolerance of V_{OUT} = ± 2%) and low power supply noise rejection (PSRR = 65dB typically)
- Drop-out voltage at 130mV (I_{OUT} = 100mA) typically
- Exceptionally small quiescent current at 0.8μA
- Outstanding line regulation (I_{OUT} = 1mA) at 0.1mV/V typically and load regulation (1mA ≤ I_{OUT} ≤ 200mA) at 0.1mV/mA typically
- Stable operation with MLCC capacitors (1.0μF / 1.0μF) of X6S & X7R types close to input & output pins over wide range of T_A from -40ºC to 125ºC
- Fault protection for over-current, short-circuit, over-temperature
- Lead-free package assembled with 'green' molding compound

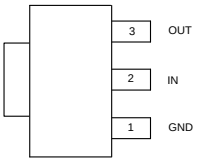
Applications

- Voltage regulation for sensitive loads like 4G/5G, WiFi, NFC
- Mainboards in FPTVs, Game Consoles, Residential Gateway, Set Top Boxes, Wearables
- Motherboards in Industrial PCs, Slot Machines, A/EIoT Gateway, Network / Communication Switches & Routers, Smart Meters

Pin Assignment

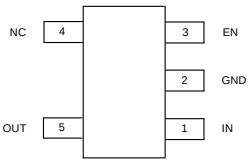
SOT-89-3L

(Top View)



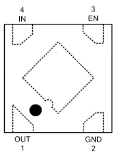
SOT-23-5L

(Top View)



DFN1010-4L

(Top View)



Ordering Information

JLR501 X X

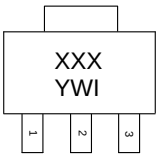
Product Prefix	Package	Output Voltage
	Y: SOT-89-3L	18: V_{OUT} = 1.8V
	S5: SOT-23-5L	28: V_{OUT} = 2.8V
	DAP: DFN1010-4L	33: V_{OUT} = 3.3V

Product Name	Package	Marking	MSL	T_J (ºC)	Media	Quantity (pcs)
JLR501DAP-18	DFN1010-4L	J018	3	-40 ~ 125	7" T&R	10,000
JLR501DAP-28		J028				
JLR501DAP-33		J033				
JLR501S5-18	SOT-23-5L	J018	3	-40 ~ 125	7" T&R	3,000
JLR501S5-28		J028				
JLR501S5-33		J033				
JLR501Y-18	SOT-89-3L	J018	3	-40 ~ 125	7" T&R	1,000
JLR501Y-28		J028				
JLR501Y-33		J033				

Marking Information

SOT-89-3L

(Top View)

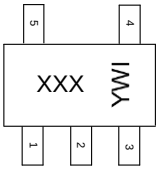


First Line: Marking (see *Ordering Information*)

Second Line: Date Code
Y: Year of Molding
W: Work-week of Molding
I: Internal Code

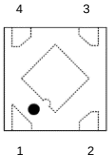
SOT-23-5L

(Top View)



DFN1010-4L

(Top View)



Typical Application Circuit

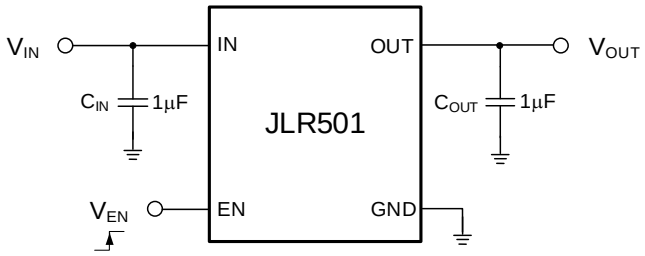


Fig. 1: Application Circuit

Notes: JLR50 is designed to work well with MLCCs. While input and output capacitors with values of ≥ 1.0μF should be populated closely between IN and GND pins, and between OUT and GND pins, high dielectric constant types with temperature characteristics X6S and X7R are preferred.

Functional Blocks

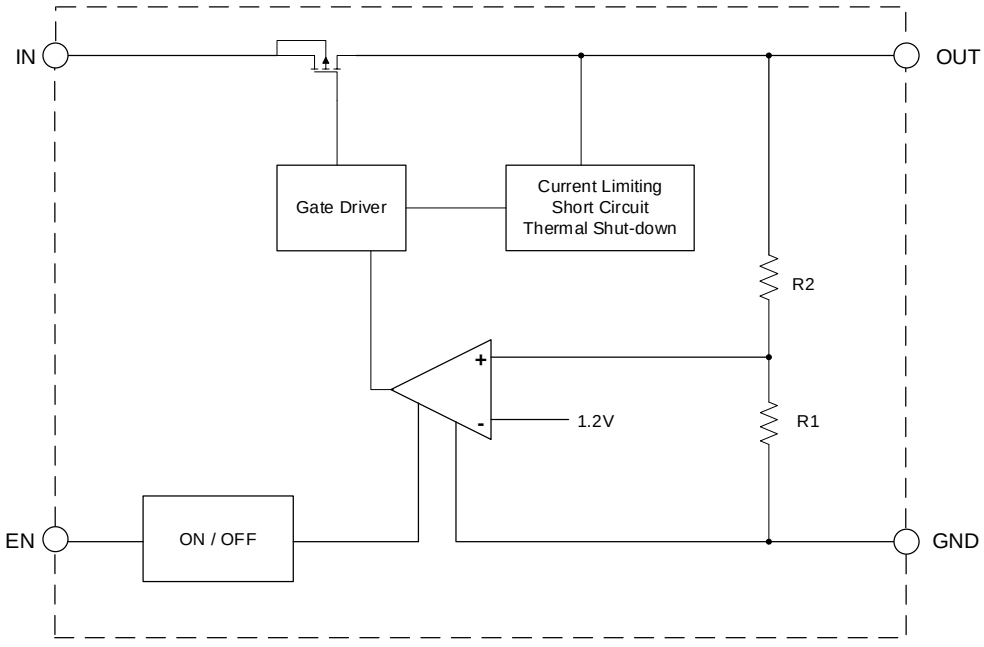


Fig. 2: Diagram of Internal Functional Blocks

Absolute Maximum Ratings *1

Symbol	Parameter	Conditions	Rating	Unit
V_{IN}	Input Voltage	-	6	V
T_J	Operating Junction Temperature	-	155	ºC
T_A	Operating Ambient Temperature	-	-40 ~ 125	ºC
T_{STG}	Storage Temperature Range	-	-40 ~ 150	ºC
P_D	Power Dissipation	SOT-23-5L	600	mW
		SOT-89-3L		
		DFN1010-4L	-	
HBM	ESD (Human Body Model)	-	4	kV
CDM	ESD (Charged Device Model)	-	0.2	kV

Notes 1: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. While these are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” are not implied. Exposure to “Absolute Maximum Ratings” over extended periods may adversely affect the device reliability.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
-	Operating Voltage Range	IN to GND	-0.3	5.5	V
		OUT to GND	-0.3	5.5	
		IN to OUT	-0.3	5.5	
		EN to GND	-0.3	5.5	
T_J	Operating Junction Temperature	-	-40	125	ºC

Electrical Characteristics

Test Conditions {V_{IN} = [V_{SET} + 1.0V] where V_{SET} = V_{OUT} @ 1.8 / 2.8 / 3.3V; C_{IN} = 1.0µF (ceramic); C_{OUT} = 1.0µF (ceramic); T_A = 25°C} are applicable to the following measurements unless otherwise stated.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating Input Voltage	-	1.2	-	5.5	V
V_{OUT}	Output Voltage	V_{IN} = 5V, I_{OUT} = 10mA	V_{SET} * 0.98	V_{SET}	V_{SET} * 1.02	V
I_{OUT}	Output Current	-	-	-	500	mA
I_Q	Quiescent Current	V_{IN} = 5V; no load	-	800	-	nA
V_{DROP}	Drop-out Voltage *2	I_{OUT} = 100mA; V_{IN} = V_{SET} - 0.1V	-	130	-	mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	V_{IN} = 4V; 1mA ≤ I_{OUT} ≤ 200mA	-	0.1	-	mV/mA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	I_{OUT} = 1mA; [V_{SET} + 2V] ≤ V_{IN} ≤ 7V	-	0.1	-	mV/V
I_{LIMIT}	Current Limit	V_{IN} = V_{SET} + 2V	-	800	-	mA
I_{SHORT}	I_{OUT} during Short-circuit	-	-	250	-	mA
V_N	Output Noise Voltage	10 ~ 100kHz; V_{IN} = V_{SET} + 2V	-	70	-	μV_{RMS}
PSRR	Power Supply Rejection Ratio	V_{IN} = 5V; I_{OUT} = 10mA; F = 1kHz	-	65	-	dB
V_{ENH}	EN Input Voltage - Logic 'H'		1.2	-	-	V
V_{ENL}	EN Input Voltage - Logic 'L'	-	-	-	0.5	V
T_{TSD}	Thermal Shut-down Threshold	Temperature rising	-	130	-	°C
		Temperature falling	-	105	-	°C

Notes 2: When the output voltage drops below its nominal value by 2%, the voltage difference between IN and OUT pins equates to V_{DROP}.

Thermal Properties

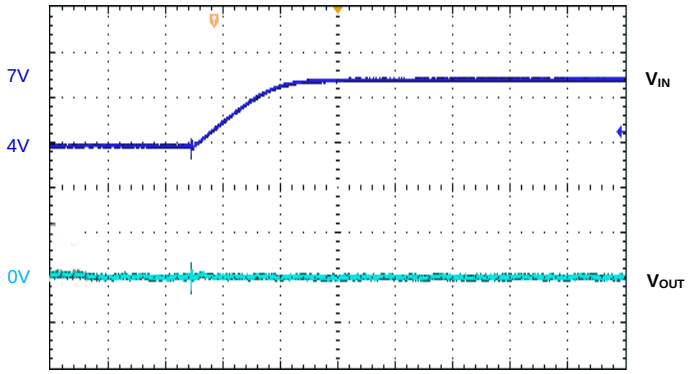
Test Conditions: Device mounted on FR-4 substrate, 2-layer PCB, 2oz copper, with minimum recommended cooling pad to dissipate heat

Symbol	Parameter	Package	Rating	Unit
$R_{\Theta JA}$	Thermal Resistance (junction-to-ambient)	SOT-23-5L	200	ºC/W
		SOT-89-3L	130	
		DFN1010-4L	300	

Performance Characteristics

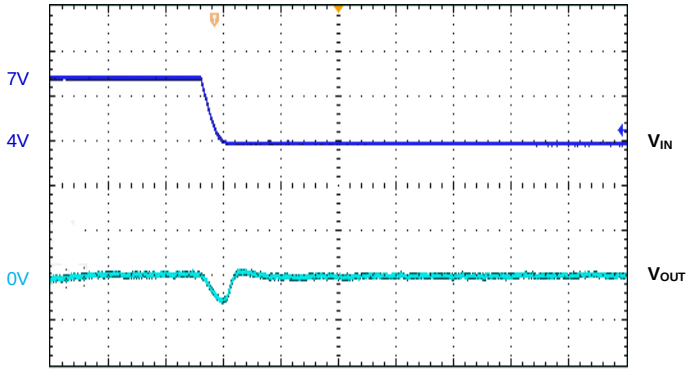
Test Conditions {V_{IN} = [V_{SET} + 1.0V] where V_{SET} = V_{OUT} @ 1.8 / 2.8 / 3.3V; C_{IN} = 1.0µF (ceramic); C_{OUT} = 1.0µF (ceramic); T_A = 25°C} are applicable to the following measurement unless otherwise stated.

Graph 1: Output Voltage vs. Input Transient ↑



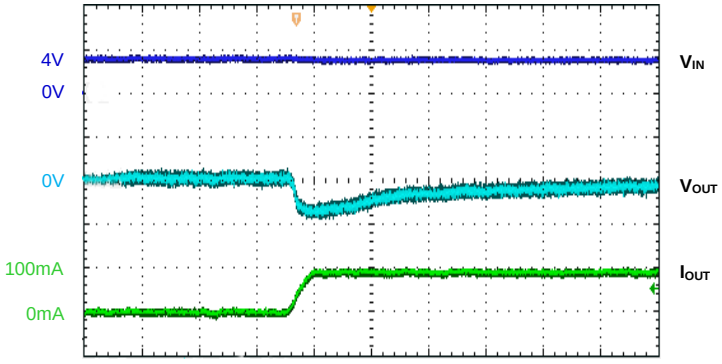
Time base @ 20 µs/div

Graph 2: Output Voltage vs. Input Transient ↓



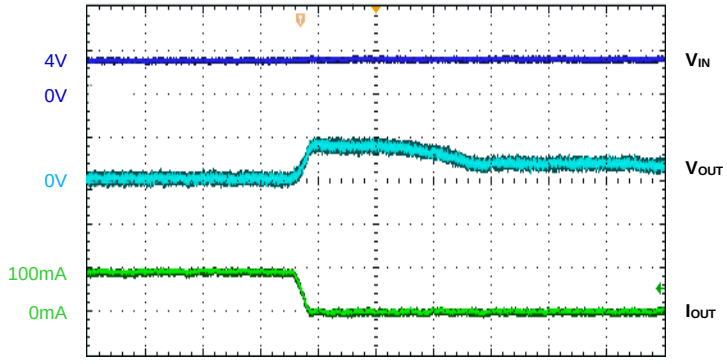
Time base @ 20 µs/div

Graph 3: Output Voltage vs. Chg. ↑ in Load Transient



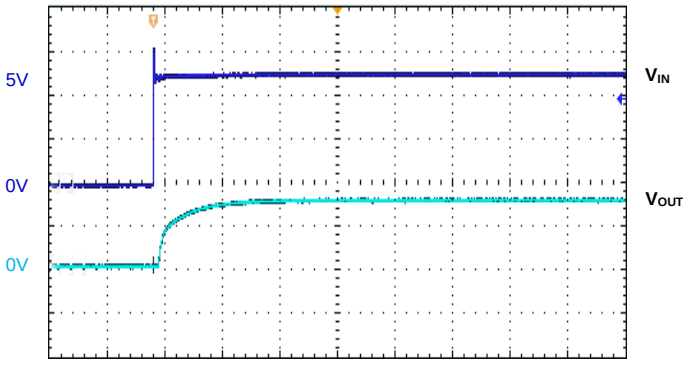
Time base @ 20 µs/div

Graph 4: Output Voltage vs. Chg. ↓ in Load Transient



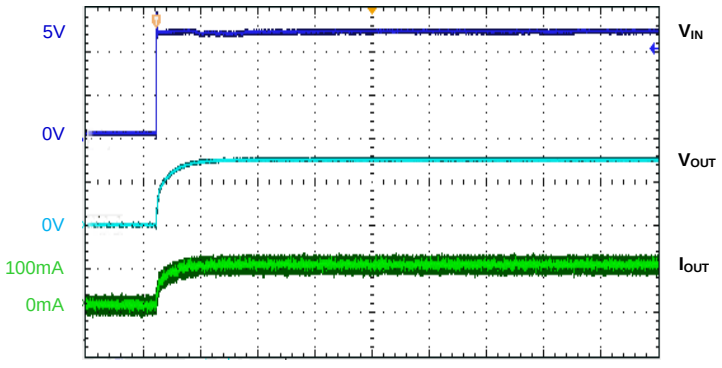
Time base @ 20 µs/div

Graph 5: No Load @ Power-ON



Time base @ 200 µs/div

Graph 6: Medium Load @ Power-ON



Time base @ 400 µs/div

Detailed Description of Device Operation

Overview

The JLR501 device is a high-performance linear regulator with input voltage up to 5.5V, and fixed output voltage levels (1.8V, 3.3V, 5.0V) at up to 500mA. It offers excellent quiescent current at 0.8μA, low drop-out voltage at 130mV, and good PSRR performance at 65dB, ultra-small quiescent current. In order to maintain reliable and consistent operation, protection features like thermal shut-down, short-circuit detection, output current limiting are built in. Further, the device responds quickly to transients over the input voltage and output loading hence over-shoot and under-shoot are minimized to lessen the adverse impact to the loading connected.

Input & Output

In order to de-couple the noise and glitch present on the power line at the input of JLR501 and the circuit board on which the device is populated, input capacitor of ceramic type with value of 1μF shall be populated as close as possible to the IN pin. Wide copper trace is required between the IN and the GND pins.

Output capacitor of ceramic type with value of 1μF shall be placed as close as possible to the OUT pin. While higher capacitance could potentially improve the load & line regulation performance and have the over-shoots and under-shoots minimized, care should be taken to ensure that the equivalent ESR do not adversely affect the high-frequency noise immunity as well as unexpected shift in phase response hence output stability.

In order to minimize the temperature dependence of the application circuit, either X6S or X7R type is recommended for both the input and output capacitors.

Current Protection

When the current appearing at the OUT pin goes up higher than the current limit designated for the device, or when the OUT & GND pins are shorted together, the built-in over-current and short-circuit protection shall be triggered. Upon the occurrence of such hazard, the output current (I_{SHORT}) shall be limited by the built-in mechanism to ~ 250mA.

Thermal Protection & Power Dissipation

When the junction temperature (T_J) of the silicon die assembled inside the device goes up beyond the normality, due either to excessive loading or short-circuit at the OUT pin, the built-in thermal shut-down protection shall be triggered. The on-die power MOSFET shall be turned OFF to prevent the device from electrical overload. Once the abnormality disappears or the junction temperature of the die comes down, the device shall resume its standard operation.

As the device operates in its typical manner, the junction temperature of the internal die goes up inevitably. Ability of the package assembly (bonding wires, lead frame, die-attach material, epoxy, etc.) to dissipate the heat generated within shall determine the overall power dissipation, P_D:

$$P_D = (V_{IN} - V_{OUT}) * I_{OUT}$$

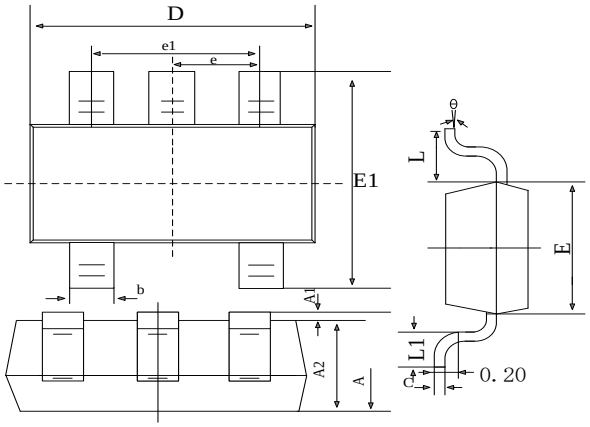
In reference to the junction-to-ambient thermal resistance ($R_{\Theta JA\_PCB}$) of the circuit board on which the device is populated, the junction temperature of the die inside the device's package can be estimated using the following equation:

$$T_J = T_A + P_D * R_{\Theta JA\_PCB}$$

The value of $R_{\Theta JA\_PCB}$ is determined, though not exclusively, by the following factors: power dissipation of the device, air flow and ambient temperature of the operating environment, PCB area, size & thickness of the copper thermal pad or the external heat sink (if any) attached, closeness of the components populated around the device, etc.

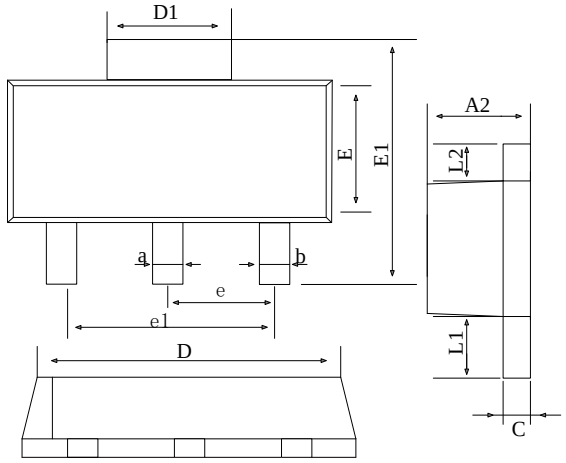
Package Outline (All measurements in mm)

Package Type: SOT-23-5L (J1)



SOT-23-5L (J1)		
Dimension	Min.	Max.
A	1.05	1.25
A1	0.00	0.10
A2	1.05	1.15
b	0.30	0.50
c	0.10	0.20
D	2.85	3.05
E	1.50	1.70
E1	2.65	2.95
e	0.95 (BSC)	
e1	1.80	2.00
L	0.30	0.60
θ	0°	8°
All measurements in "mm"		

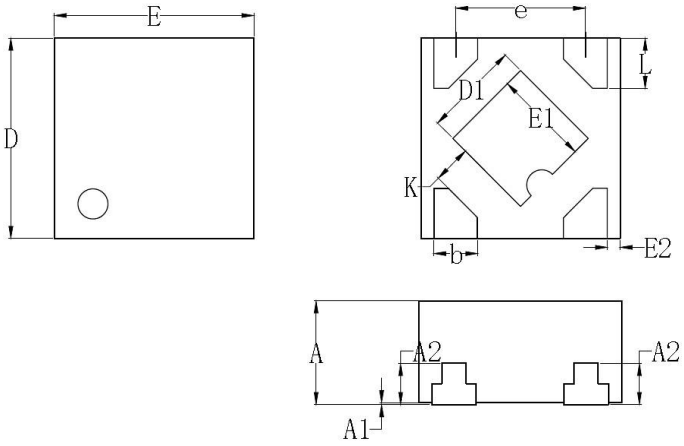
Package Type: SOT-89-3L (J1)



SOT-89-3L (J1)		
Dimension	Min.	Max.
A	1.40	1.60
a	0.45	0.55
b	0.38	0.48
c	0.36	0.46
D	4.40	4.60
D1	1.60	1.80
E	2.40	2.60
E1	4.00	4.30
e	1.00	2.00
e1	2.95	3.05
L	0.80	1.00
L2	0.65	0.75
All measurements in "mm"		

Package Outline (All measurements in mm)

Package Type: DFN1010-4L (J1)



DFN1010-4L (J1)			
Dimension	Min.	Typ.	Max.
A	0.45	0.50	0.55
	0.50	0.55	0.60
A1	0.00	-	0.05
A2		0.203 TIY	
b	0.17	0.22	0.27
D	0.95	1.00	1.05
D1	0.43	0.48	0.53
E	0.95	1.00	1.05
E1	0.43	0.48	0.53
E2		0.065 TIY	
e		0.650 BSC	
K		0.200 BSC	
L	0.20	0.25	0.30
All measurements in "mm"			

Disclaimer

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