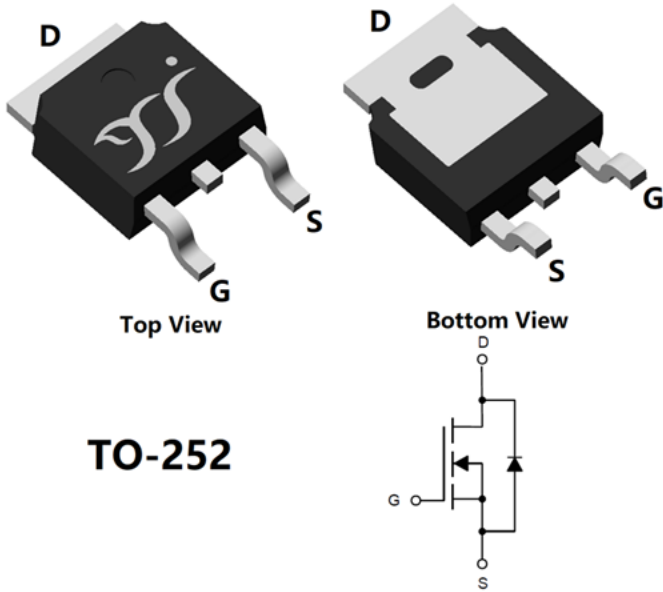


N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 250V
- I_D 8A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<470m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

■ Absolute Maximum Ratings ($T_J=25^\circ C$ unless otherwise noted)

Parameter			Symbol	Limit	Unit
Drain-source Voltage			V_{DS}	250	V
Gate-source Voltage			V_{GS}	± 30	V
Continuous Drain Current (Note 1,2)	Steady-State	$T_A=25^\circ C$	I_D	1.5	A
		$T_A=100^\circ C$		0.9	
Continuous Drain Current (Note 1,3)	Steady-State	$T_C=25^\circ C$		8	
		$T_C=100^\circ C$		5	
Pulsed Drain Current	$T_C=25^\circ C, t_p=100\mu s$		I_{DM}	25	A
Avalanche energy			EAS	21.16	mJ
Total Power Dissipation (Note 1,2)	Steady-State	$T_A=25^\circ C$	P_D	2.5	W
		$T_A=100^\circ C$		1	
Total Power Dissipation (Note 1,3)	Steady-State	$T_C=25^\circ C$		69	
		$T_C=100^\circ C$		27	
Junction and Storage Temperature Range			T_J, T_{STG}	-55~+150	$^\circ C$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	40	50	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.5	1.8	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD470N25H	F1/F2	YJD470N25H	2500	/	25000	13"Reel



YJD470N25H

■ Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	250	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V$	-	-	1	μA
		$V_{DS}=40V, V_{GS}=0V, T_J=150^\circ\text{C}$	-	-	100	
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 30V, V_{DS}=0V$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.2	3	3.8	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=4A$	-	300	470	m Ω
Diode Forward Voltage	V_{SD}	$I_S=8A, V_{GS}=0V$	-	-	1.2	V
Gate resistance	R_G	$f=1\text{MHz}$	-	3	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	8	A
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=125V, V_{GS}=0V, f=1\text{MHz}$	-	715	-	μF
Output Capacitance	C_{oss}		-	39	-	
Reverse Transfer Capacitance	C_{rss}		-	3.4	-	
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=10V, V_{DS}=125V, I_D=4A$	-	13.8	-	nC
Gate-Source Charge	Q_{gs}		-	3.4	-	
Gate-Drain Charge	Q_{gd}		-	4.8	-	
Reverse Recovery Charge	Q_{rr}	$I_F=4A, di/dt=100A/\mu s$	-	346	-	nC
Reverse Recovery Time	t_{rr}		-	84	-	ns
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DD}=125V, I_D=4A$ $R_{GEN}=2.7\Omega$	-	20	-	ns
Turn-on Rise Time	t_r		-	6.9	-	
Turn-off Delay Time	$t_{D(off)}$		-	16.4	-	
Turn-off fall Time	t_f		-	12	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $T_A=25^\circ\text{C}$. The maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.
- Thermal resistance from junction to soldering point (on the exposed drain pad).



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Typical Electrical and Thermal Characteristics Diagrams

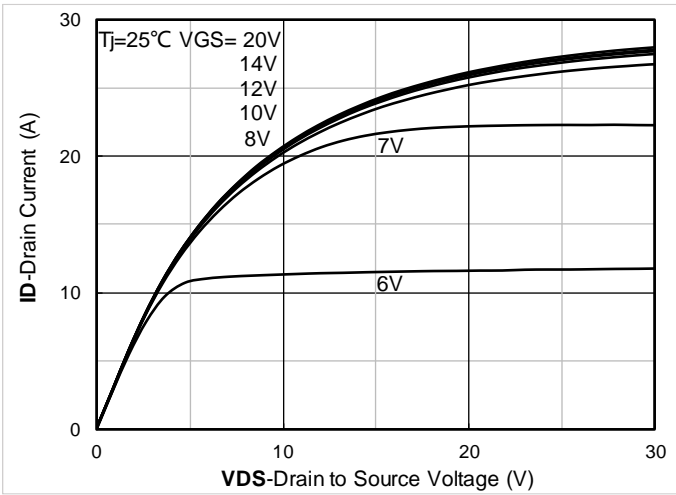


Figure 1. Output Characteristics

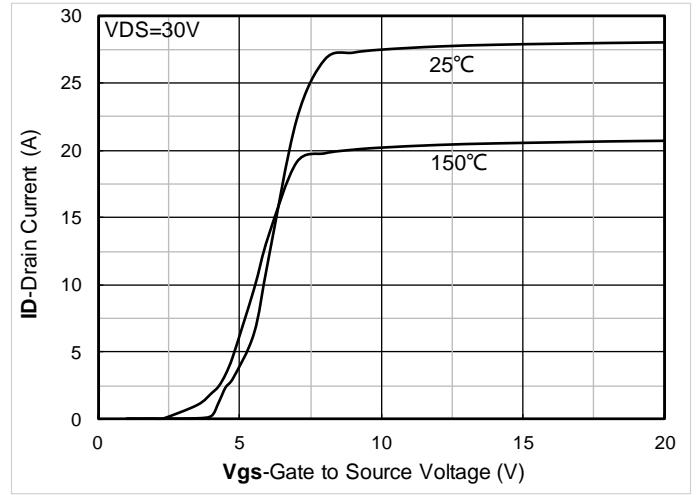


Figure 2. Transfer Characteristics

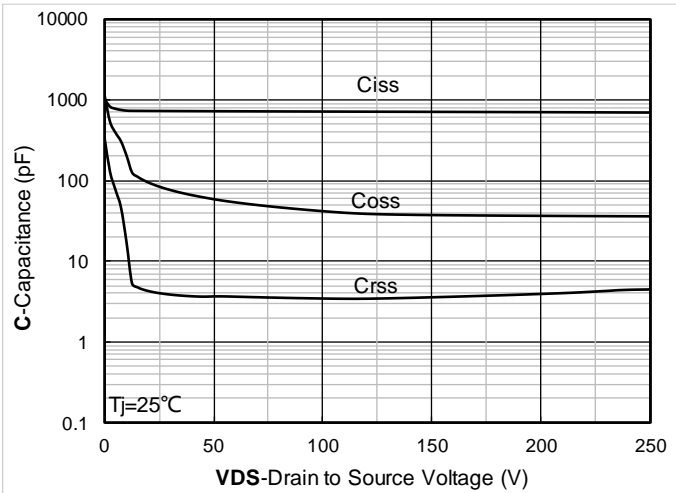


Figure 3. Capacitance Characteristics

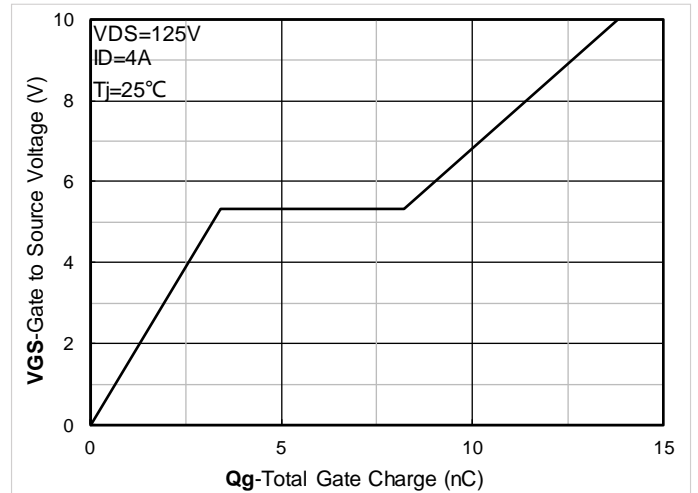


Figure 4. Gate Charge

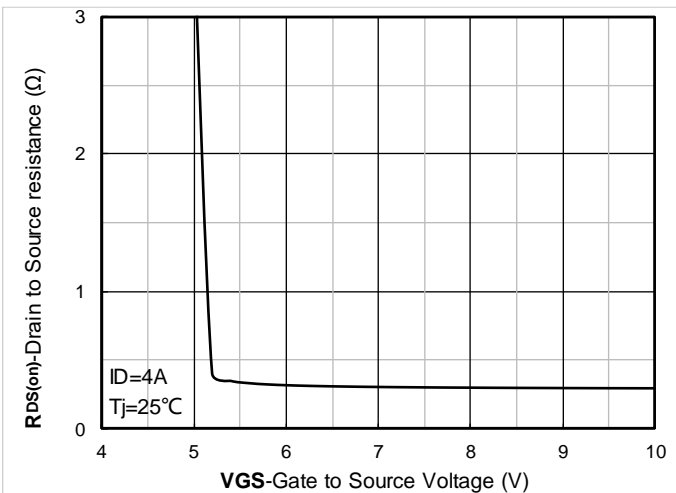


Figure 5. On-Resistance vs Gate to Source Voltage

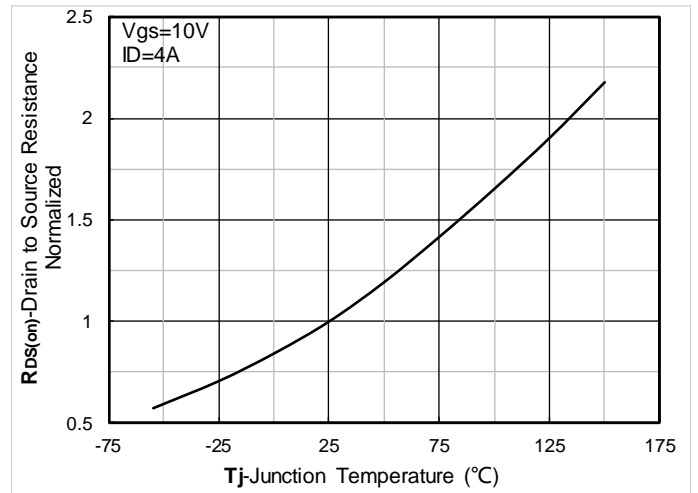


Figure 6. Normalized On-Resistance



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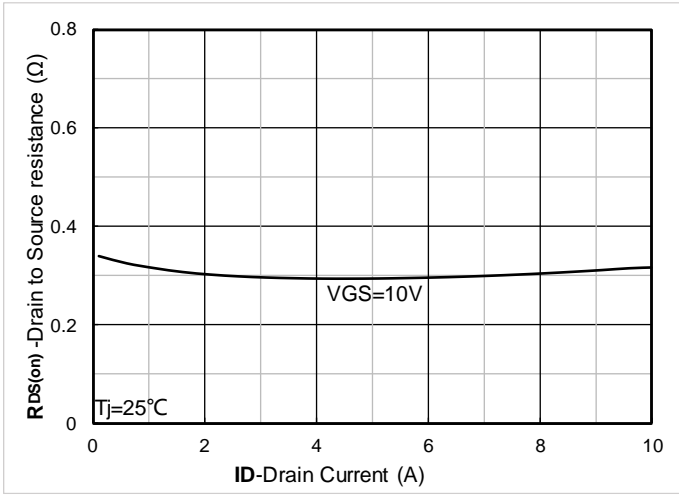


Figure 7. RDS(on) VS Drain Current

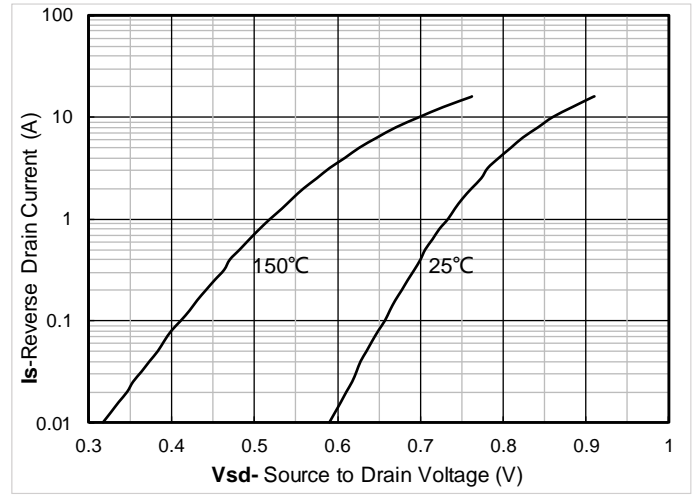


Figure 8. Forward characteristics of reverse diode

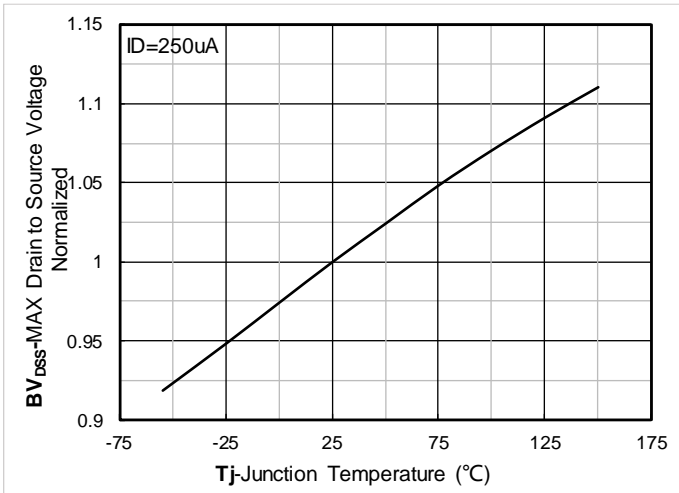


Figure 9. Normalized breakdown voltage

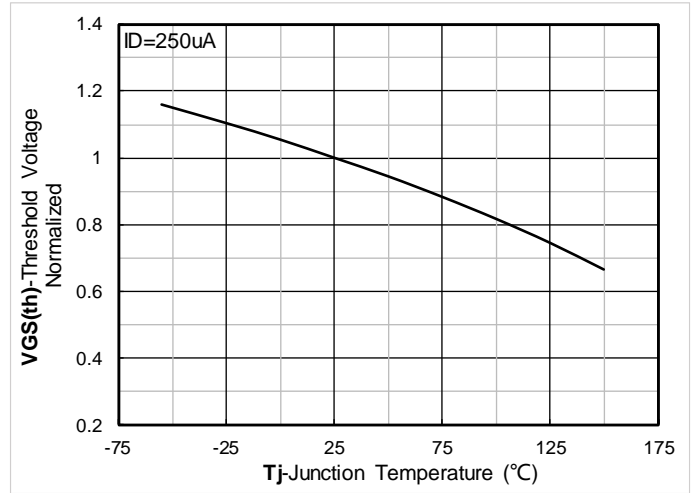


Figure 10. Normalized Threshold voltage

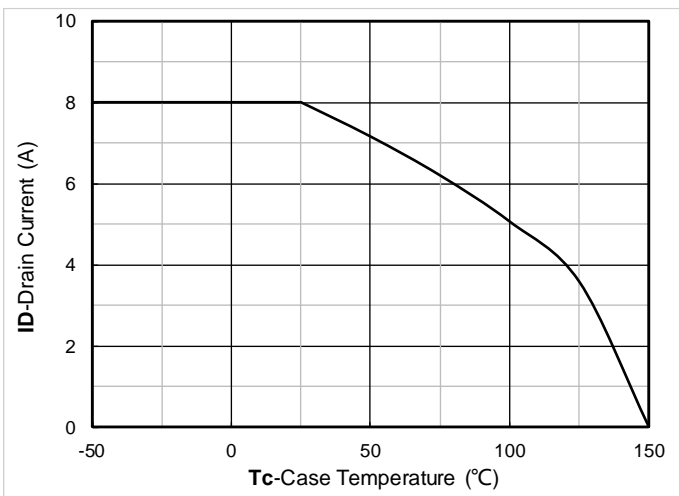


Figure 11. Current dissipation

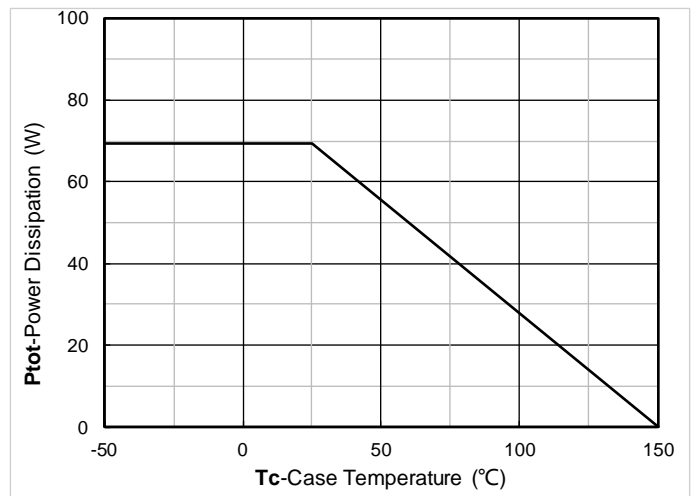


Figure 12. Power dissipation

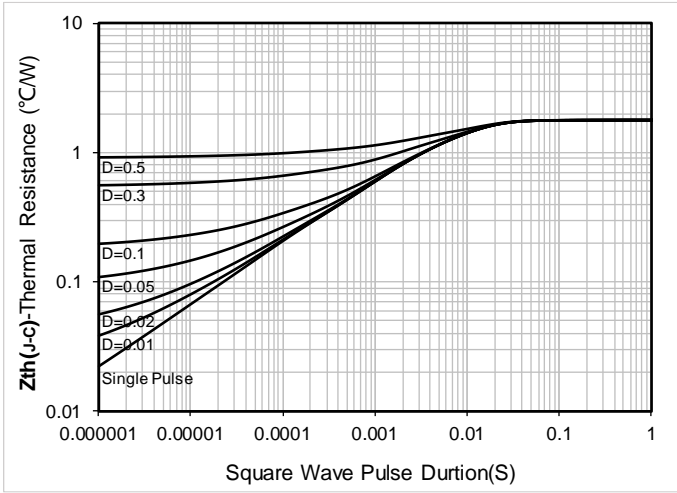


Figure 13. Maximum Transient Thermal Impedance

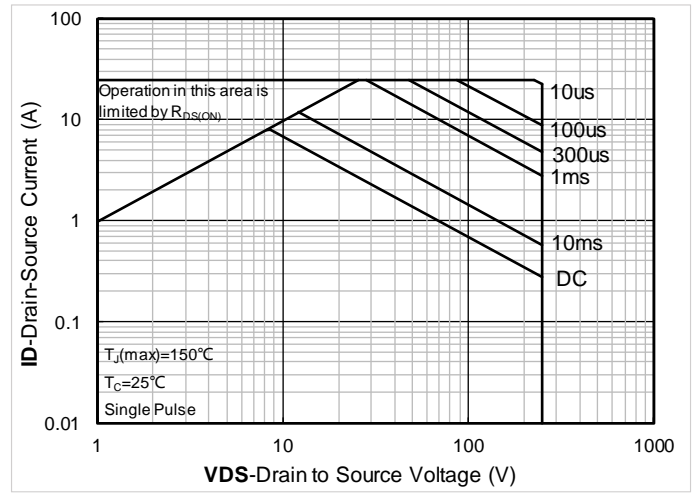


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

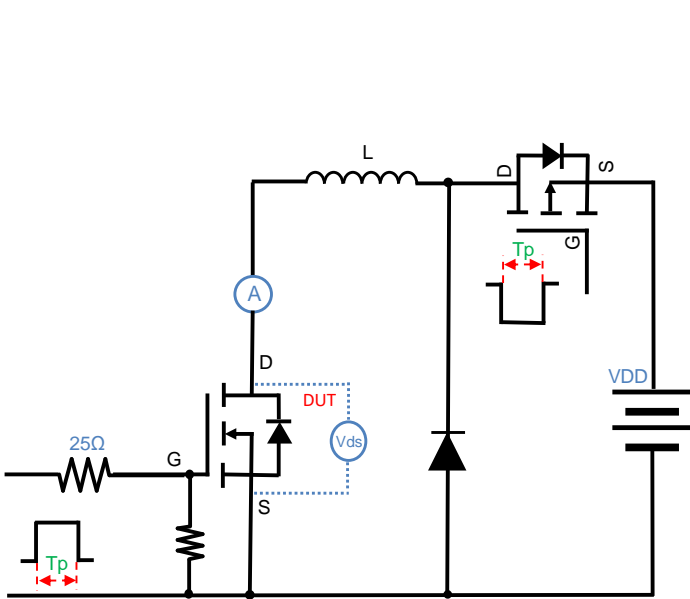
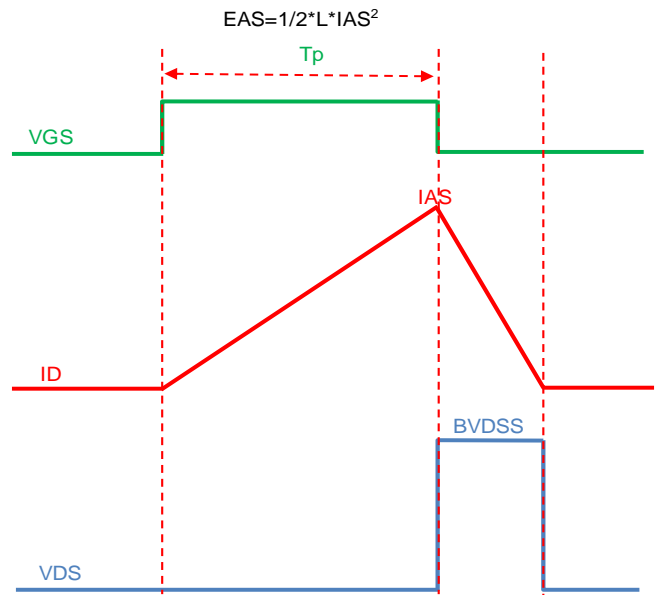


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform



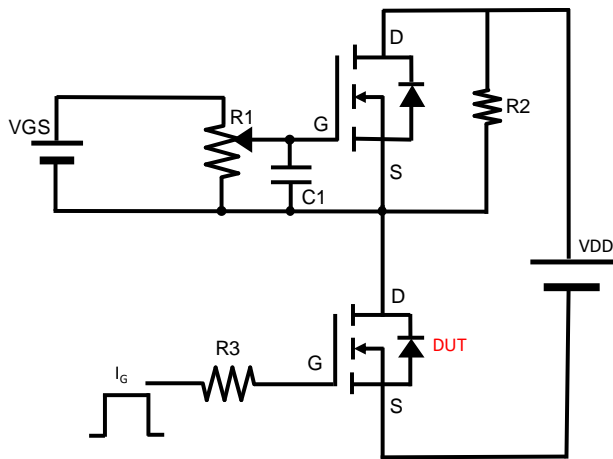


Figure B. Gate Charge Test Circuit & Waveform

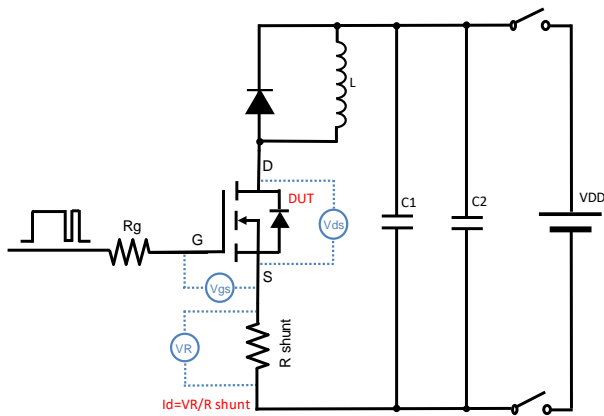


Figure C. Resistive Switching Test Circuit & Waveform

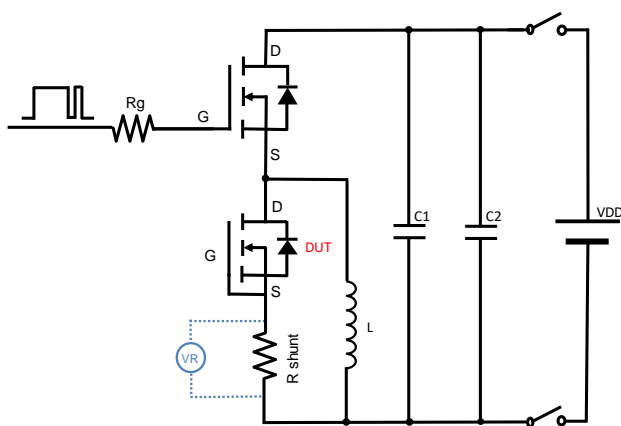
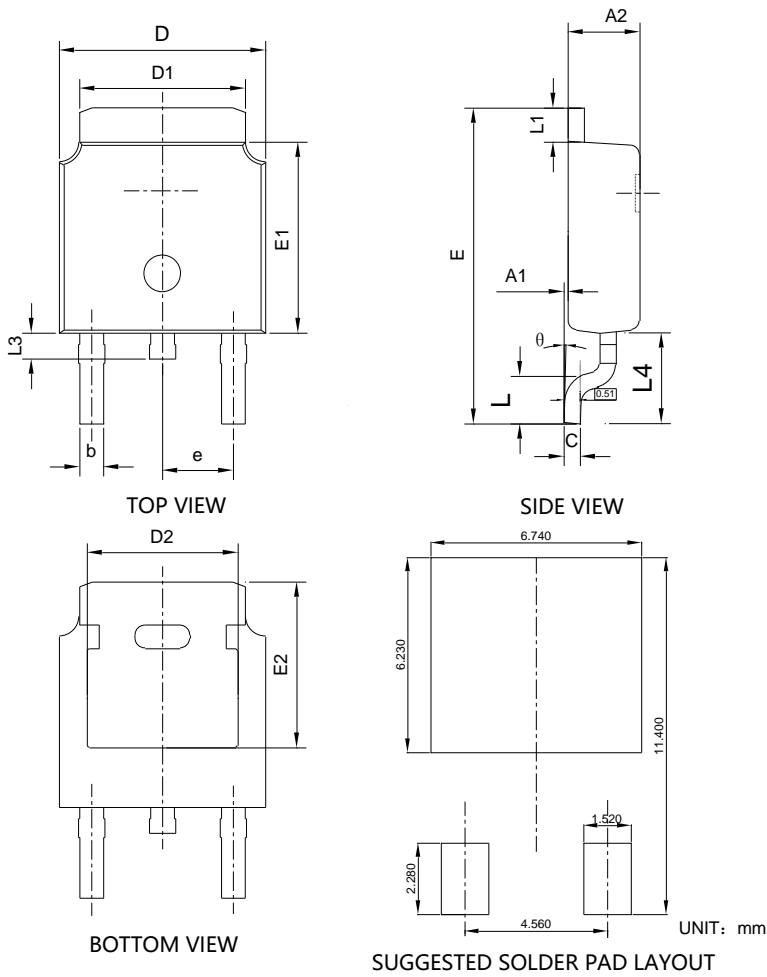


Figure D. Diode Recovery Test Circuit & Waveform



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■ TO-252-C Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A1	0.000	0.008	0.000	0.200
A2	0.086	0.094	2.180	2.400
b	0.026	0.035	0.660	0.890
c	0.018	0.024	0.460	0.610
D	0.250	0.265	6.350	6.730
D1	0.195	0.215	4.950	5.460
D2	0.170	-	4.320	-
E	0.370	0.410	9.400	10.410
E1	0.235	0.245	5.970	6.220
E2	0.203	-	5.150	-
e	0.090 REF		2.286 REF	
L	0.049	0.070	1.250	1.780
L1	0.035	0.050	0.890	1.270
L3	0.024	0.039	0.600	1.000
L4	0.102	0.126	2.600	3.200
θ	0°	10°	0°	10°

NOTE:
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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