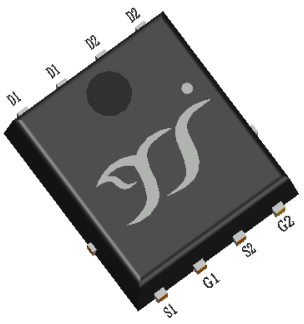
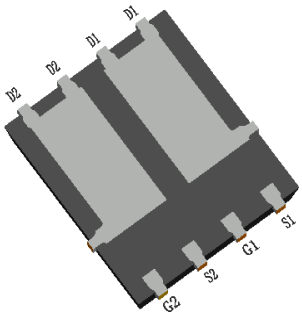
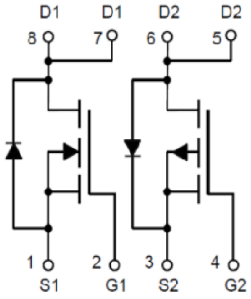
N-Channel and P-Channel Complementary MOSFET





PDFN5060-8L



Product Summary

NMOS

- V_{DS} 100V
- I_D 40A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜24mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜30mΩ
- 100% EAS Tested
- 100% ▽V_{DS} Tested

PMOS

- V_{DS} -100V
- I_D -12A
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜115mΩ
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜138mΩ
- 100% EAS Tested
- 100% ▽V_{DS} Tested

General Description

- Excellent package for heat dissipation
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

■ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Parameter		Symbol	NMOS	PMOS	Unit
Drain-source Voltage		V_{DS}	100	-100	V
Gate-source Voltage		V_{GS}	±20	±20	V
Drain Current	T_A=25℃	I_D	7.5	-3.3	A
	T_A=100℃		4.7	-2.0	
	T_C=25℃		40	-12	
	T_C =100℃		25	-7.6	
Pulsed Drain Current [A]		I_{DM}	80	-40	A
Avalanche energy [B]		EAS	72	36	mJ
Total Power Dissipation [C]	T_A=25℃	P_D	2.5	2.5	W
	T_A=100℃		1	1	
	T_C=25℃		104	69	
	T_C =100℃		41	27	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	-55～+150	℃

■Thermal resistance

Parameter		Symbol	NMOS		PMOS		Units
			Typ	Max	Typ	Max	
Thermal Resistance Junction-to-Ambient [D]	Steady-State	$R_{\theta JA}$	40	50	40	50	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1	1.2	1.5	1.8	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG12NP10BQ	F1	YJG12NP10B	5000	10000	100000	13“ reel

■ NMOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.2	1.7	2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	16	24	mΩ
		V_{GS}=4.5V, I_D=5A	-	18	30	
Diode Forward Voltage	V_{SD}	I_S=20A, V_{GS}=0V	-	0.9	1.3	V
Gate resistance	R_G	f=1MHz	-	1.5	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1MHz	-	1270	-	pF
Output Capacitance	C_{oss}		-	750	-	
Reverse Transfer Capacitance	C_{rss}		-	35	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=20A		17	-	nC
Gate-Source Charge	Q_{gs}			6	-	
Gate-Drain Charge	Q_{gd}			3	-	
Reverse Recovery Charge	Q_{rr}	I_F=20A, di/dt=100A/us		42	-	nC
Reverse Recovery Time	t_{rr}			40	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=50V,I_D=20A R_{GEN}=3.0Ω		40	-	ns
Turn-on Rise Time	t_r			12	-	
Turn-off Delay Time	$t_{D(off)}$			55	-	
Turn-off fall Time	t_f			16	-	

■ PMOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	-100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V, V_{GS}=0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-1.2	-1.7	-2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-12A	-	85	115	mΩ
		V_{GS}=-4.5V, I_D=-3A	-	92	138	
Diode Forward Voltage	V_{SD}	I_S=-12A, V_{GS}=0V	-	-0.9	-1.2	V
Gate resistance	R_G	f=1MHz	-	10	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-25V, V_{GS}=0V, f=1MHz	-	1120	-	pF
Output Capacitance	C_{oss}		-	180	-	
Reverse Transfer Capacitance	C_{rss}		-	25	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V, V_{DS}=-50V, I_D=-6A	-	20	-	nC
Gate-Source Charge	Q_{gs}		-	4	-	
Gate-Drain Charge	Q_{gd}		-	4.5	-	
Reverse Recovery Charge	Q_{rr}	I_F=-6A, di/dt=100A/us	-	140	-	nC
Reverse Recovery Time	t_{rr}		-	70	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V, V_{DD}=-50V, ID=-6A RGEN=2.2Ω	-	10	-	ns
Turn-on Rise Time	t_r		-	30	-	
Turn-off Delay Time	$t_{D(off)}$		-	77	-	
Turn-off fall Time	t_f		-	80	-	

A. Repetitive rating; pulse width limited by max. junction temperature.
B. NMOS: T_J=25℃, V_{DD}=50V, V_G=10V, R_G=25Ω, L=0.5mH, IAS=17A. PMOS: T_J=25℃, V_{DD}=-50V, V_G=-10V, R_G=25Ω, L=0.5mH, IAS=-12A.
C. P_d is based on max. junction temperature, using junction-case thermal resistance.
D. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in the still air environment with T_A =25℃. The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.

■ NMOS Typical Electrical and Thermal Characteristics Diagrams

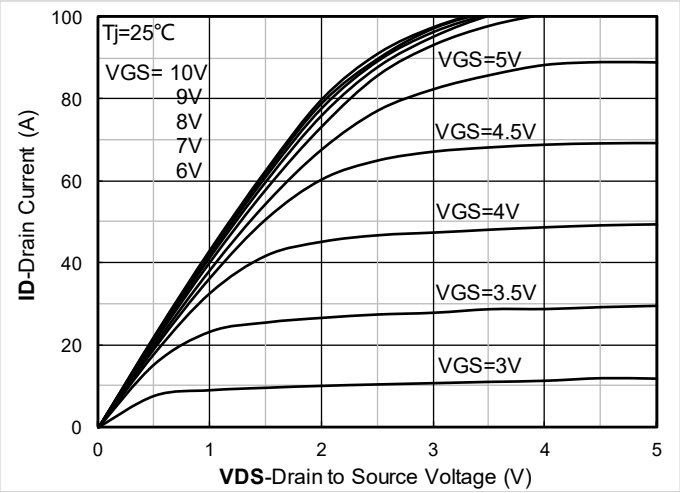


Figure 1. Output Characteristics

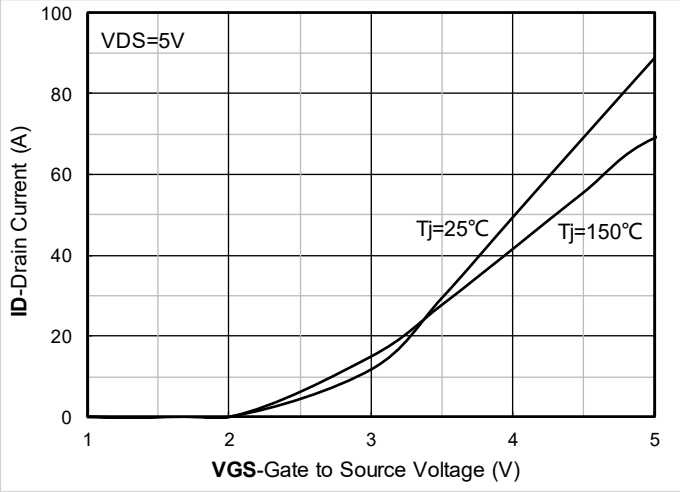


Figure 2. Transfer Characteristics

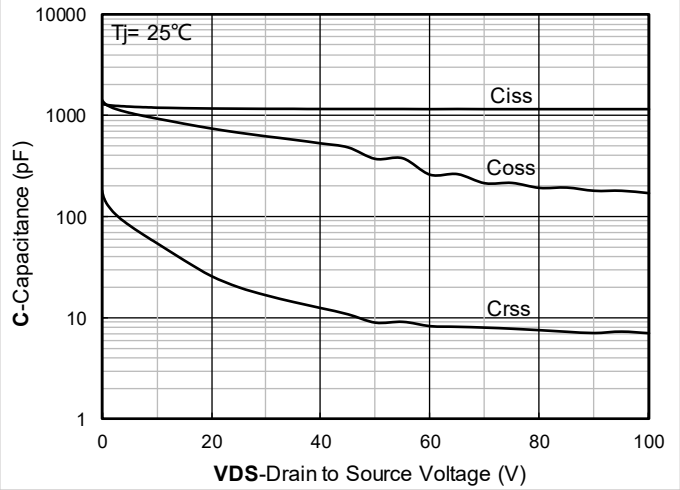


Figure 3. Capacitance Characteristics

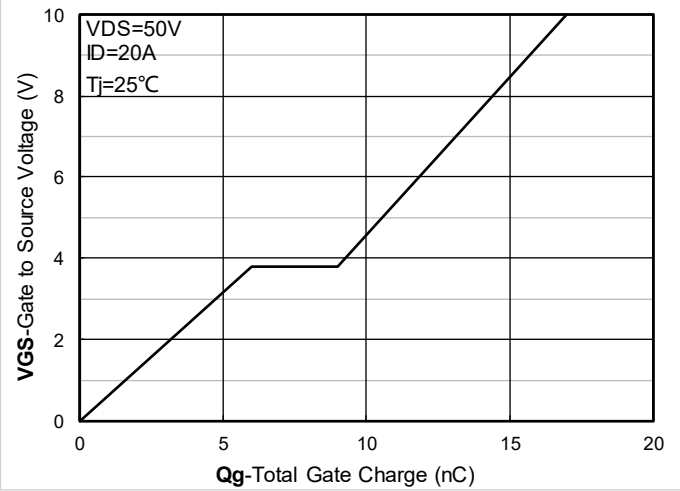


Figure 4. Gate Charge

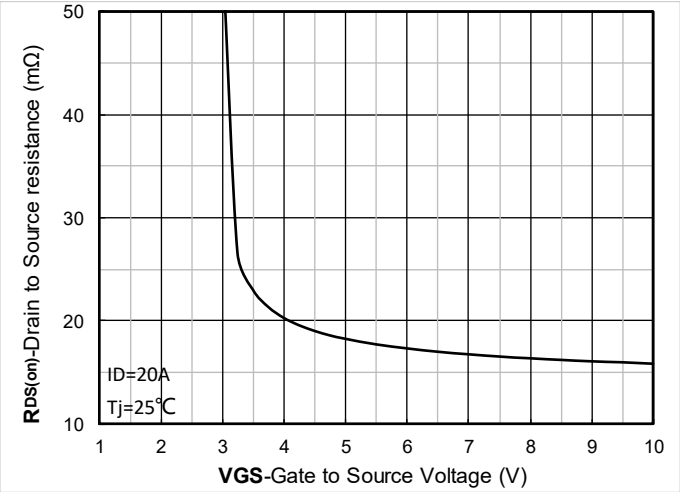


Figure 5. On-Resistance vs Gate to Source Voltage

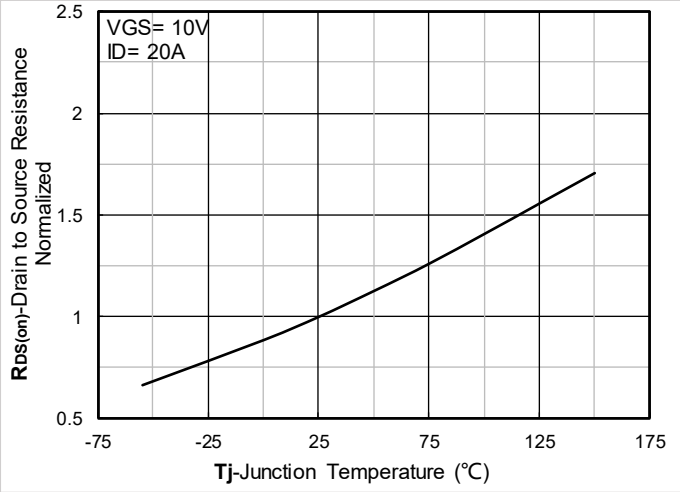


Figure 6. Normalized On-Resistan

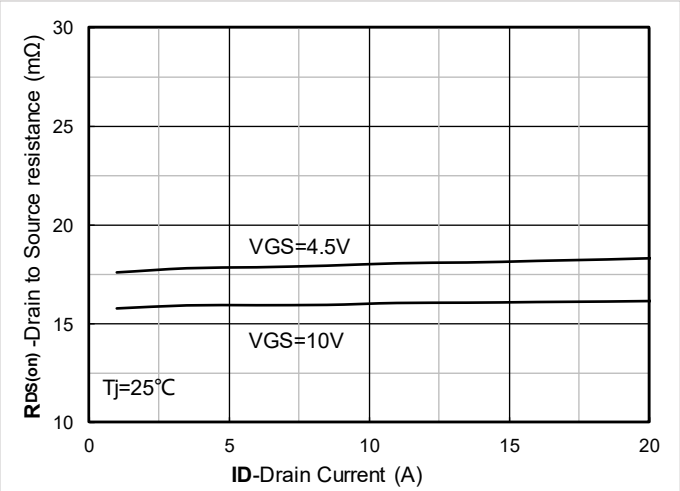


Figure 7. $R_{DS(on)}$ VS Drain Current

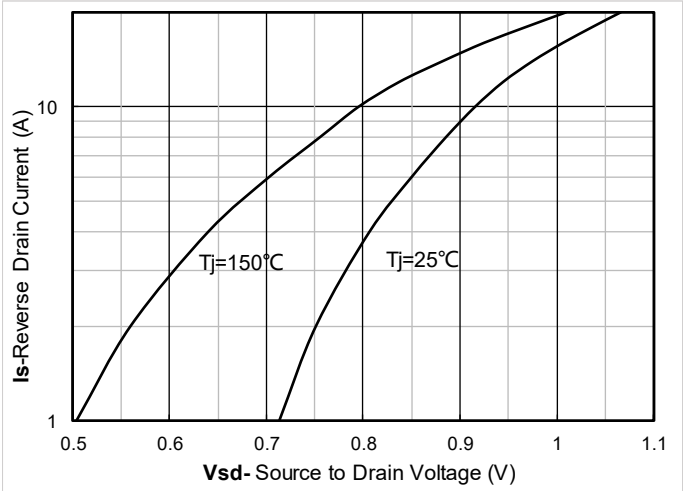


Figure 8. Forward characteristics of reverse diode

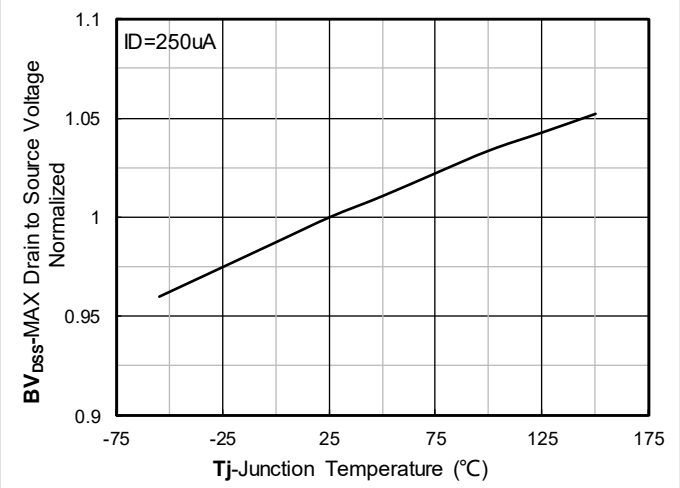


Figure 9. Normalized breakdown voltage

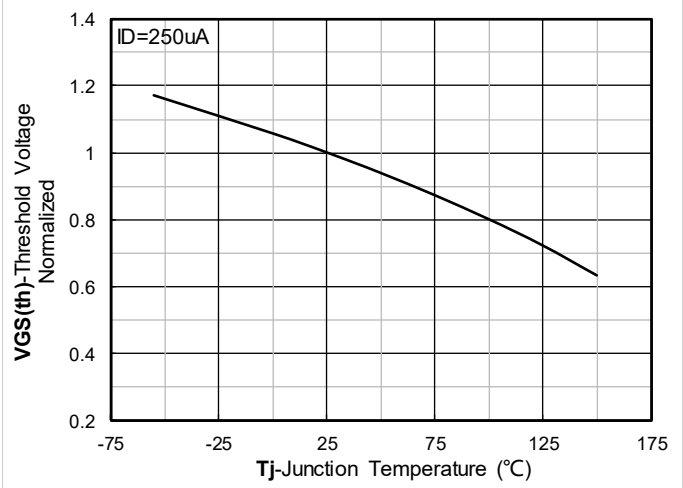


Figure 10. Normalized Threshold voltage

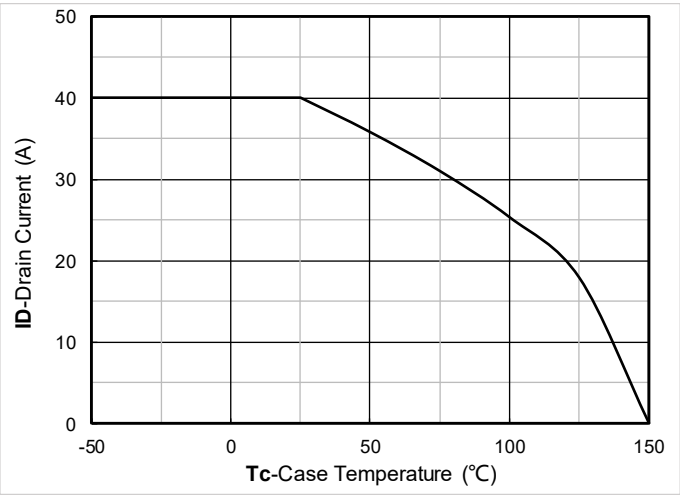


Figure 11. Current dissipation

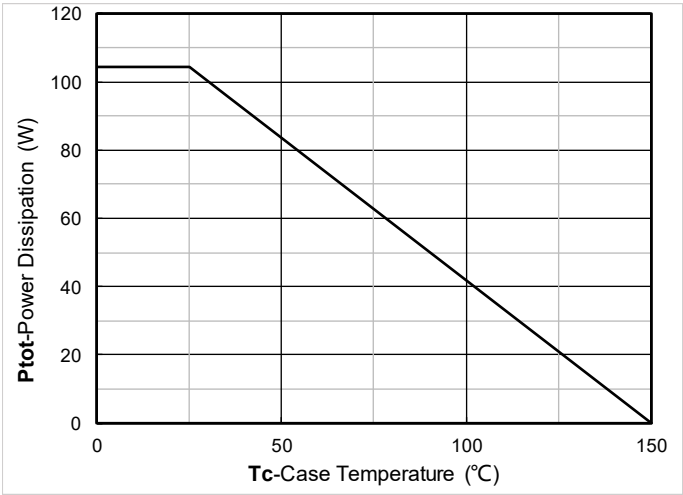


Figure 12. Power dissipation

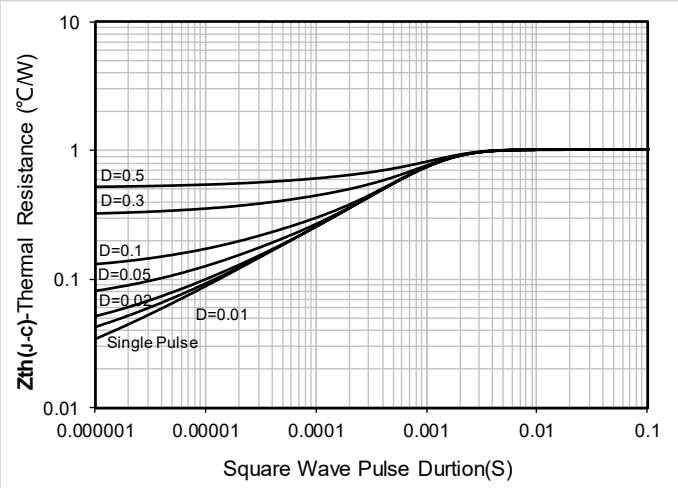


Figure 13. Maximum Transient Thermal Impedance

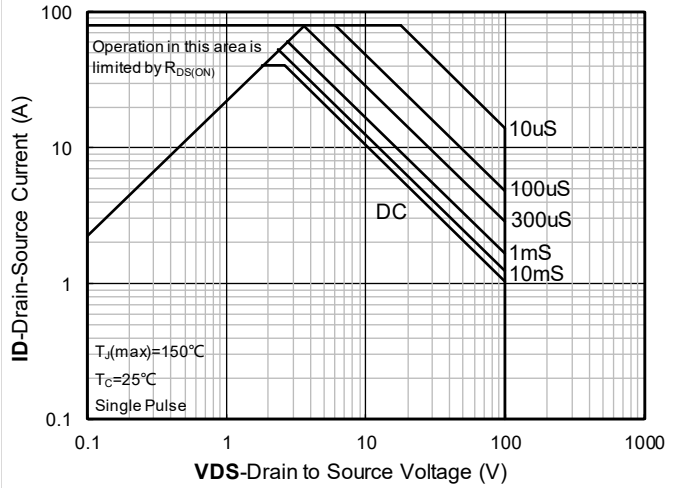


Figure 14. Safe Operation Area

■ PMOS Typical Electrical and Thermal Characteristics Diagrams

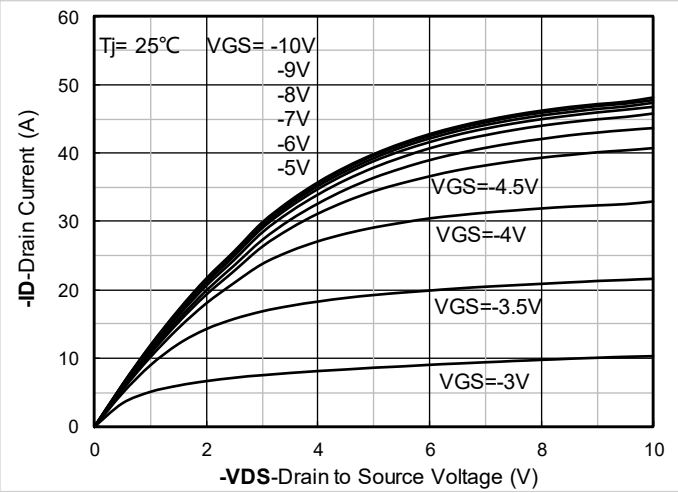


Figure 1. Output Characteristics

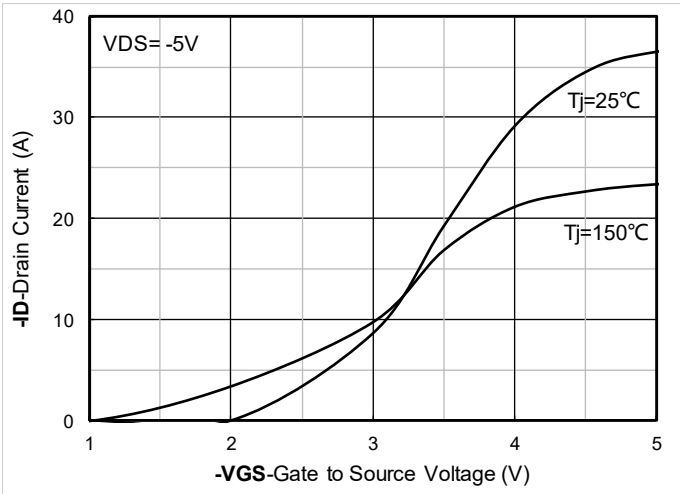


Figure 2. Transfer Characteristics

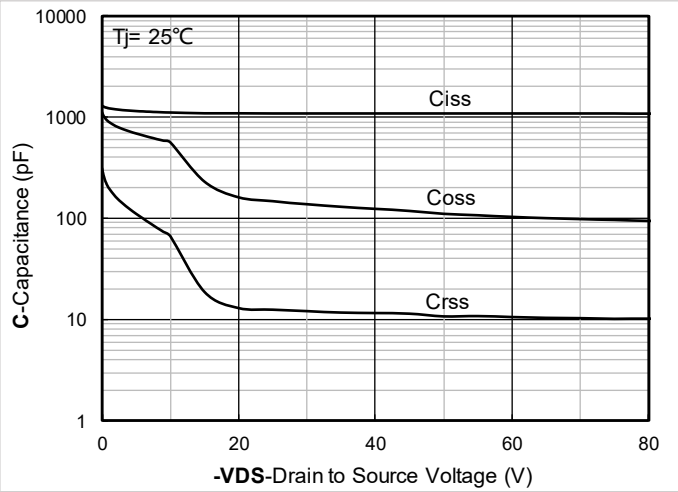


Figure 3. Capacitance Characteristics

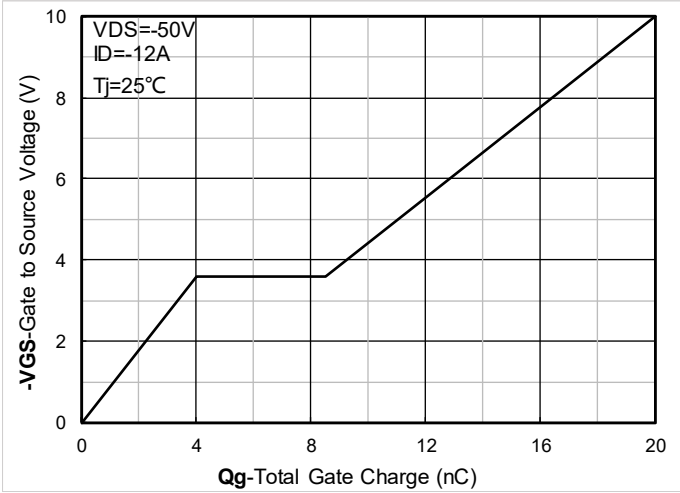


Figure 4. Gate Charge

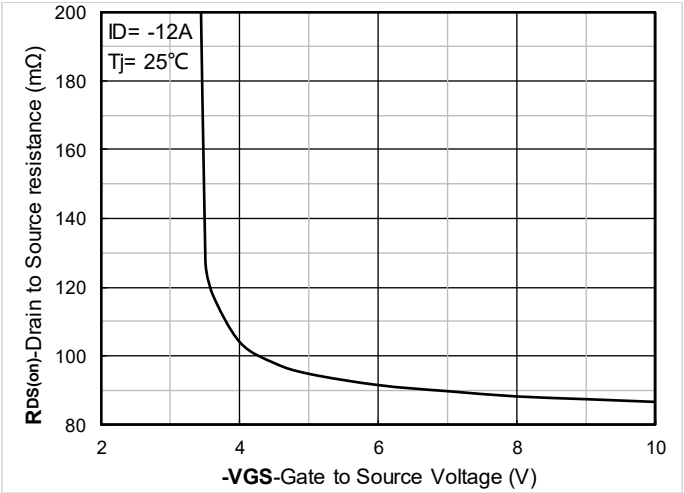


Figure 5. On-Resistance vs Gate to Source Voltage

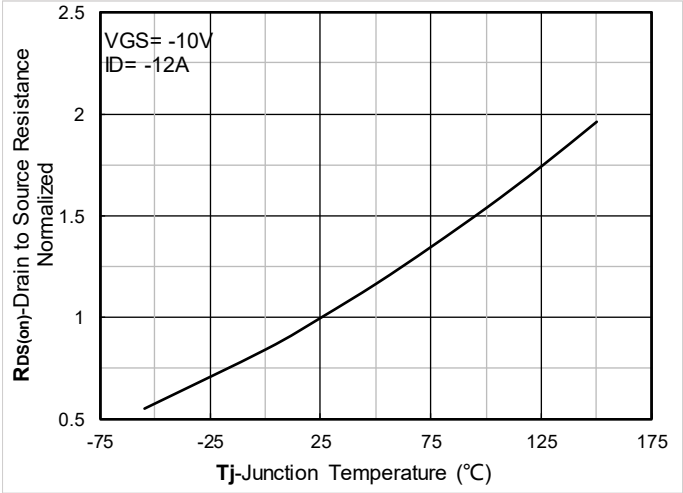


Figure 6. Normalized On-Resistance

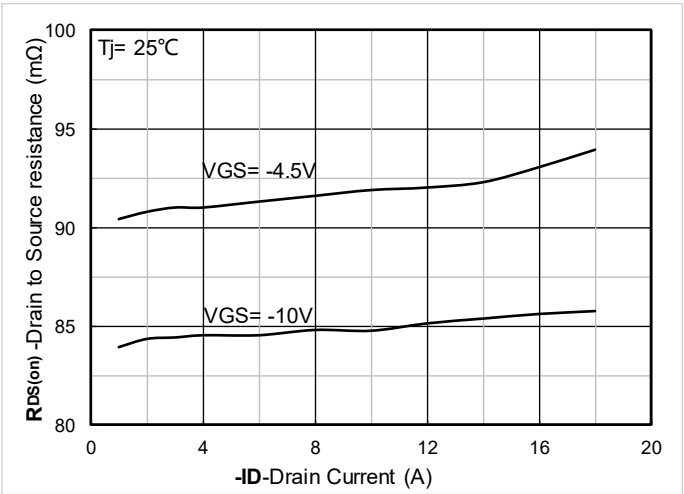


Figure 7. $R_{DS(on)}$ VS Drain Current

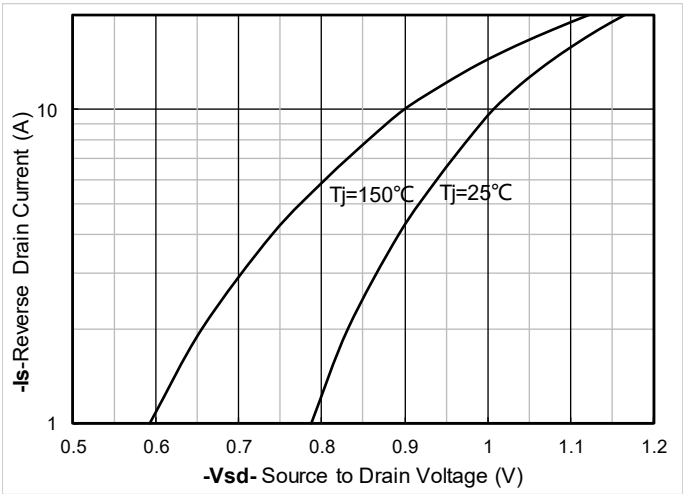


Figure 8. Forward characteristics of reverse diode

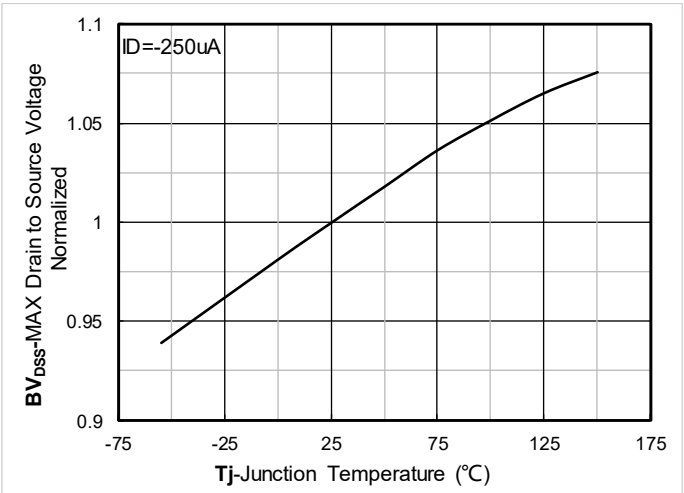


Figure 9. Normalized breakdown voltage

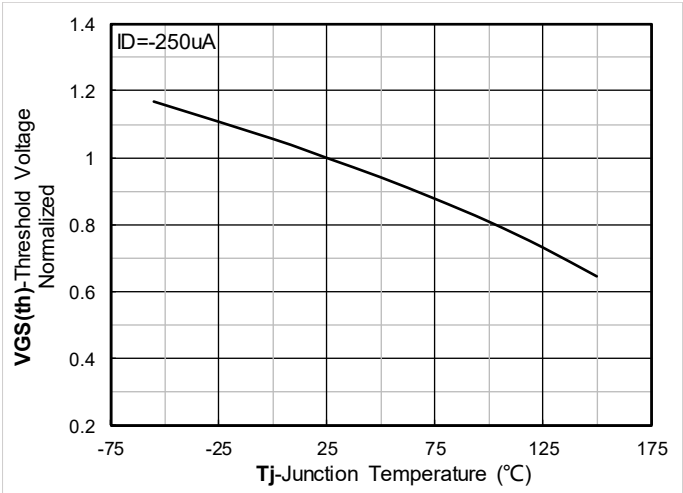


Figure 10. Normalized Threshold voltage

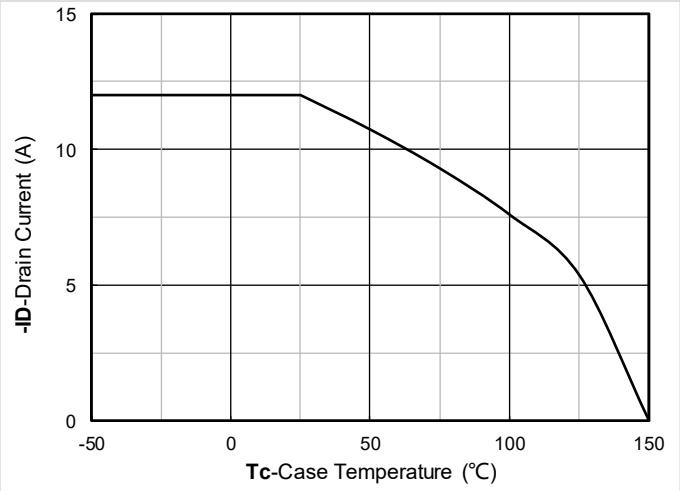


Figure 11. Current dissipation

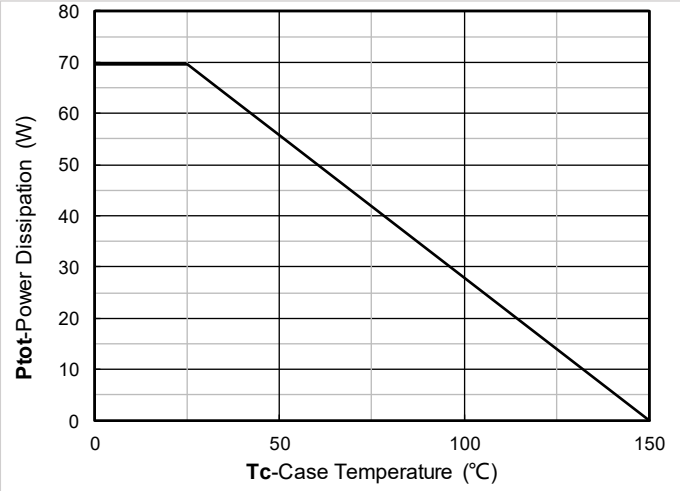


Figure 12. Power dissipation

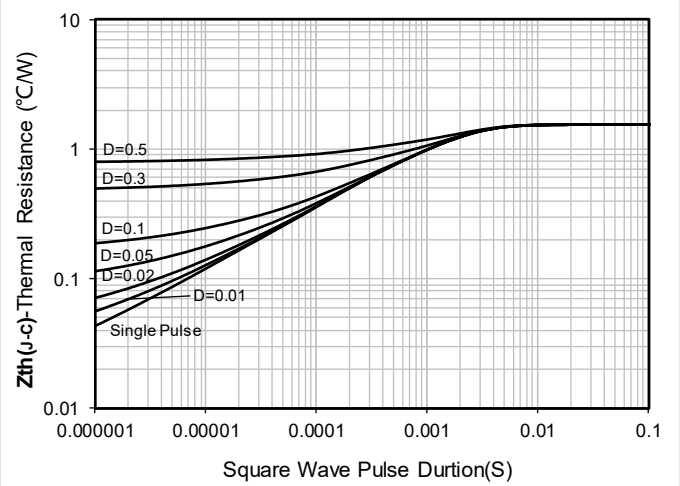


Figure 13. Maximum Transient Thermal Impedance

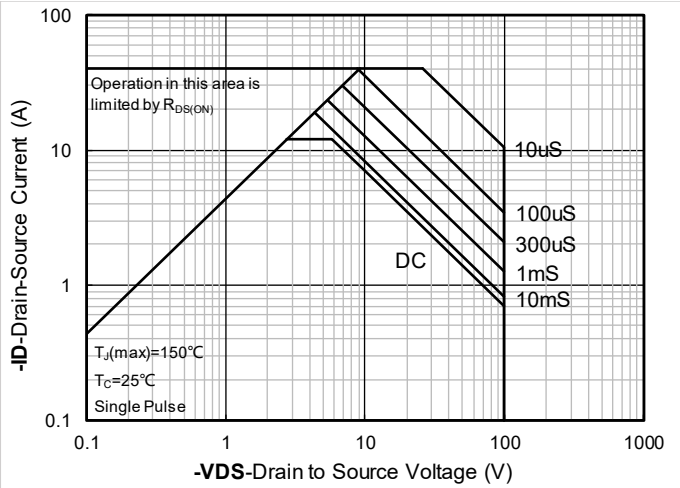
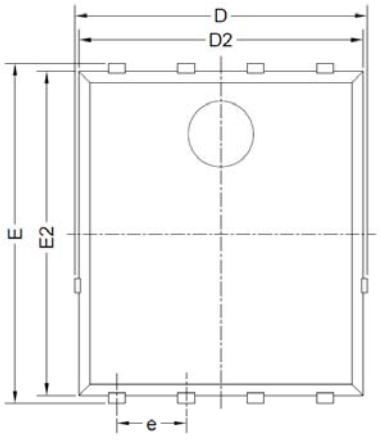
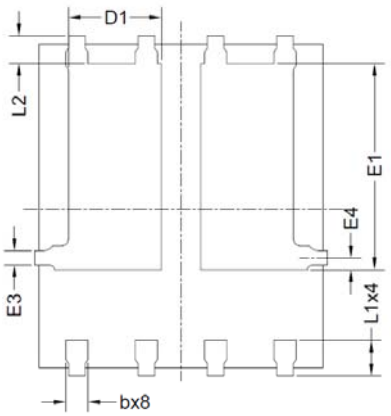


Figure 14. Safe Operation Area

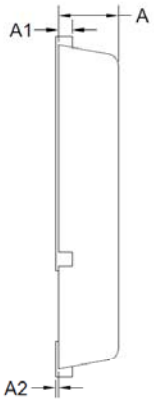
■ PDFN5060-8L Package information



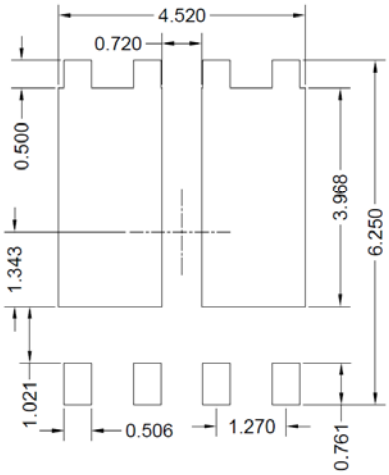
Top View
正面视图



Bottom View
背面视图



Side View
侧面视图



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	1.50	1.70	1.90
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3		0.254REF	
E4		0.21REF	
L1	0.56	0.66	0.76
L2		0.50 BSC	
b	0.31	0.41	0.51
e		1.27 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

Disclaimer

The information presented in this document is for reference only. Yangzhou Yangjie Electronic Technology Co., Ltd. reserves the right to make changes without notice for the specification of the products displayed herein to improve reliability, function or design or otherwise.

The product listed herein is designed to be used with automotive electronics,are not designed for use in medical, life-saving, lifesustaining,or military,Yangjie or anyone on its behalf, assumes no responsibility or liability for any damages resulting from such improper use of sale.

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