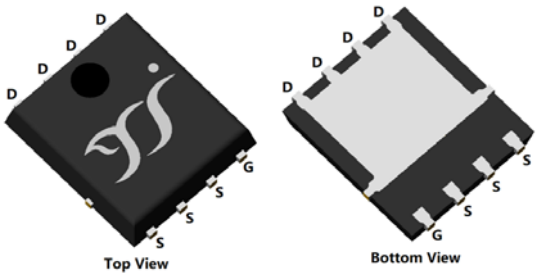
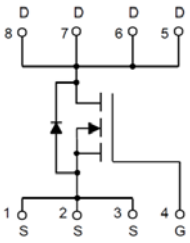
N-Channel Enhancement Mode Field Effect Transistor



PDFN5060-8L



Product Summary

- V_{DS} 100V
- I_D 60A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜12 mohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜15 mohm
- 100% UIS Tested
- 100% ▽VDS Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- High Frequency Switching
- Synchronous Rectification
- 12V, 24V and 48V Automotive systems

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	Tc=25℃	I_D	60	A
	Tc=125℃		28	
Pulsed Drain Current [A]		I_{DM}	240	A
Avalanche energy [B]		EAS	200	mJ
Total Power Dissipation [C]	Tc=25℃	P_D	78	W
	Tc=125℃		15	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [D]	Steady-State	$R_{\theta JA}$	92	100	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.3	1.6	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG60G10BQ	F1	YJG60G10B	5000	10000	100000	13" reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1	1.8	2.8	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A		8.0	12	mΩ
		V_{GS}=4.5V, I_D=20A		9.5	15	mΩ
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V			1.3	V
Maximum Body-Diode Continuous Current	I_S				60	A
Gate resistance	R_G	f=1MHz, Open drain		1		Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V,f=1MHZ		2500		pF
Output Capacitance	C_{oss}			1385		
Reverse Transfer Capacitance	C_{rss}			45		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=13V,V_{DS}=50V,I_D=30A		36.0		nC
Gate-Source Charge	Q_{gs}			6.3		
Gate-Drain Charge	Q_{gd}			13.8		
Reverse Recovery Chrage	Q_{rr}	V_{GS}=0V,di/dt=100A/us,I_S=30A		280		
Reverse Recovery Time	t_{rr}			10.5		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=13V,V_{DD}=50V,I_{DS}=30A R_{GEN}=2.3Ω		12		
Turn-on Rise Time	t_r			62		
Turn-off Delay Time	$t_{D(off)}$			24.5		
Turn-off fall Time	t_f			3.5		

A. Repetitive rating; pulse width limited by max. junction temperature.
B. V_{DD}=50V, R_G=25Ω, L=1mH, IAS=20A
C. P_d is based on max. junction temperature, using junction-case thermal resistance.
D. The value of $R_{\theta JA}$ is measured with the device mounted on the minimum recommend pad size, in the still air environment with T_A =25℃.
The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.

■ Typical Performance Characteristics

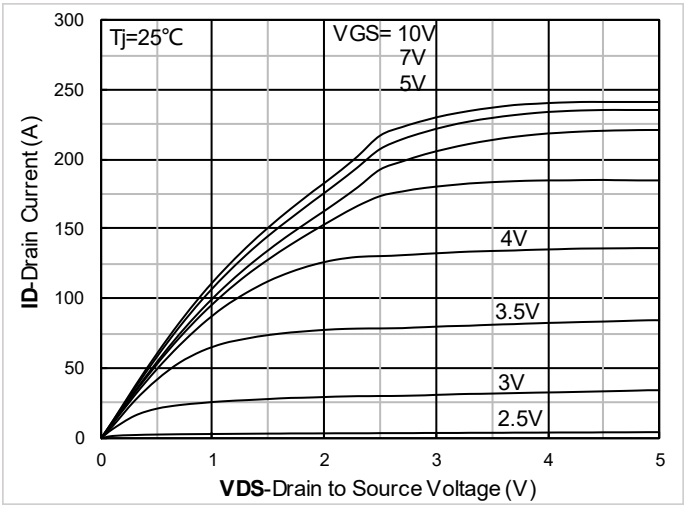


Figure 1. Output Characteristics

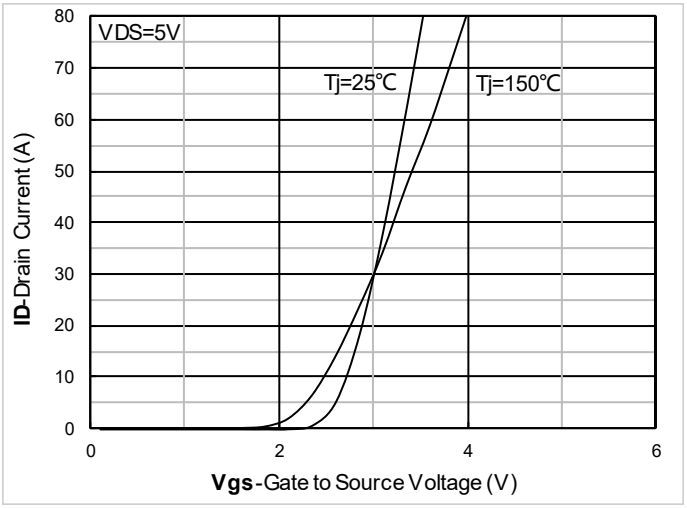


Figure 2. Transfer Characteristics

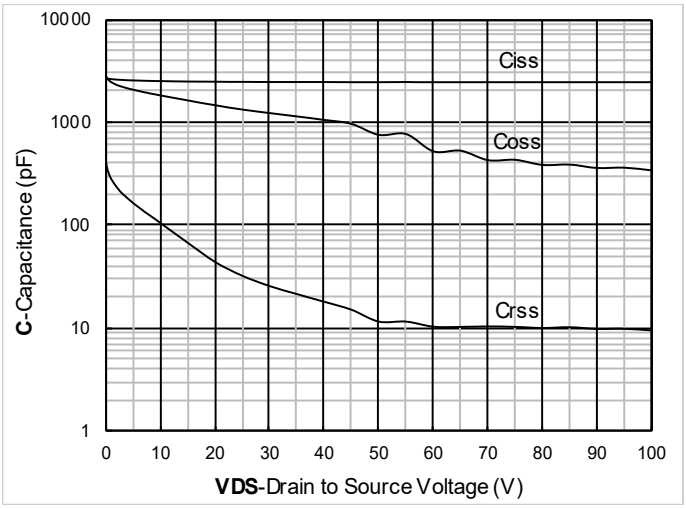


Figure 3. Capacitance Characteristics

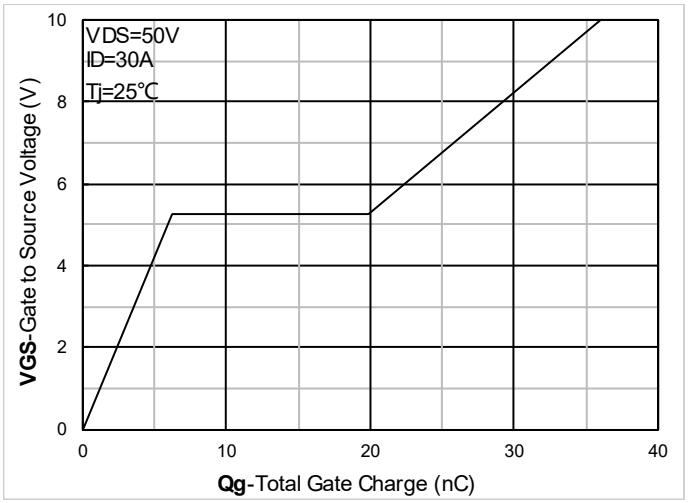


Figure 4. Gate Charge

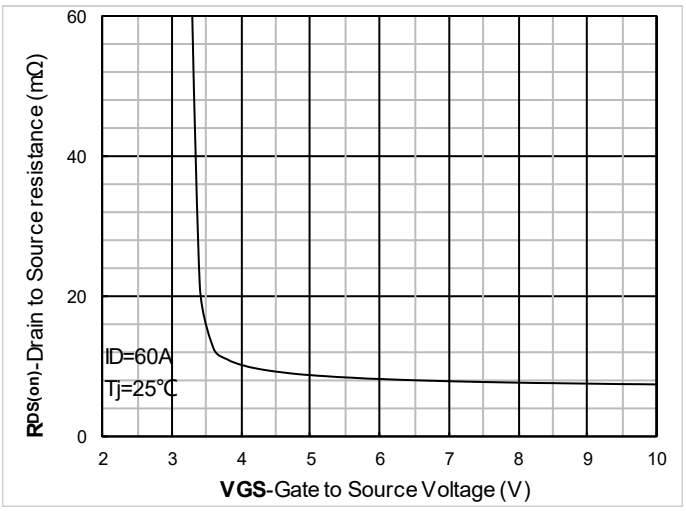


Figure 5. On-Resistance vs Gate to Source Voltage

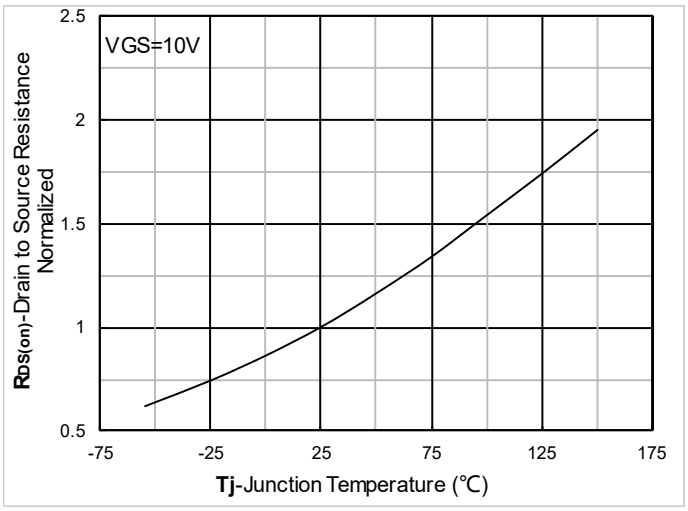


Figure 6. Normalized On-Resistance

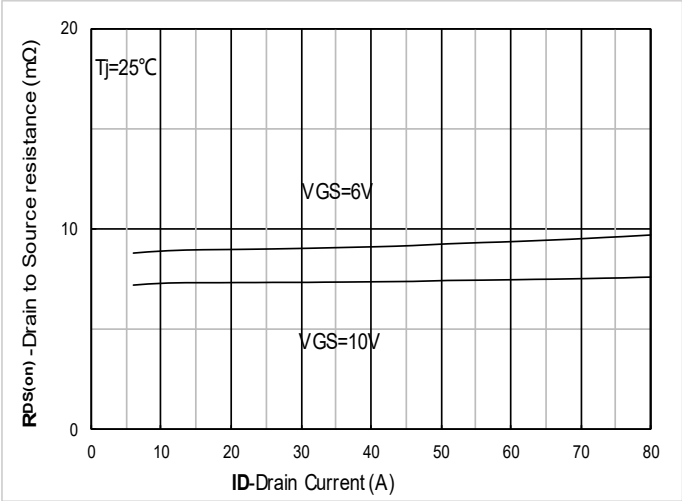


Figure 7. $R_{DS(on)}$ VS Drain Current

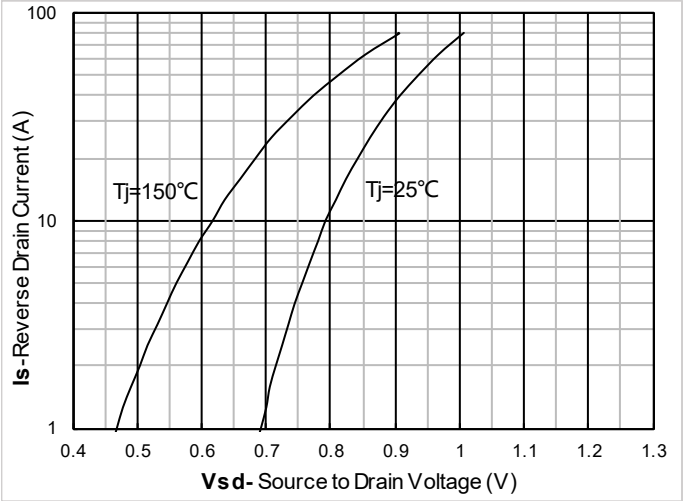


Figure 8. Forward characteristics of reverse diode

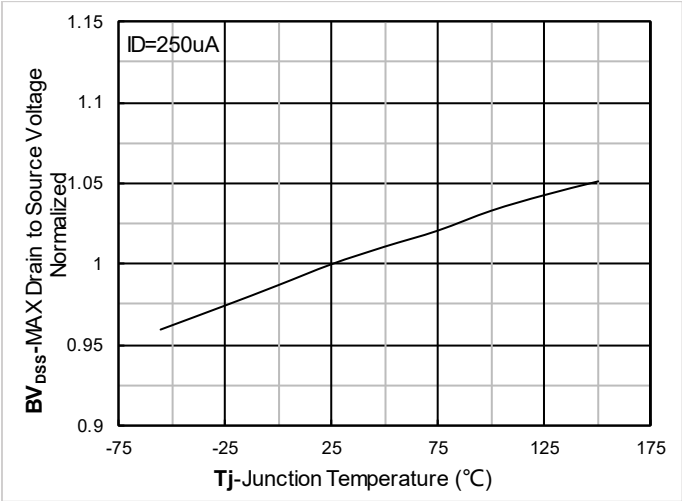


Figure 9. Normalized breakdown voltage

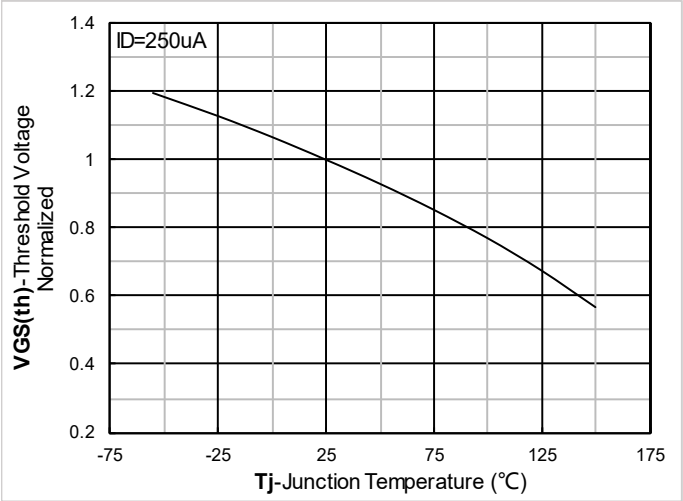


Figure 10. Normalized Threshold voltage

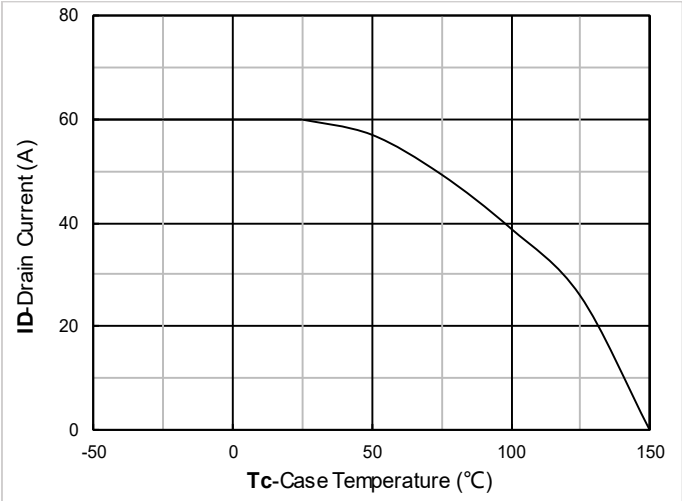


Figure 11. Current dissipation

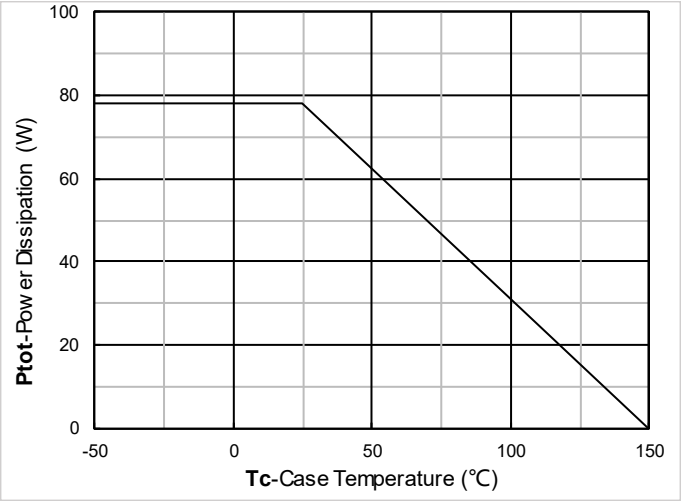


Figure 12. Power dissipation

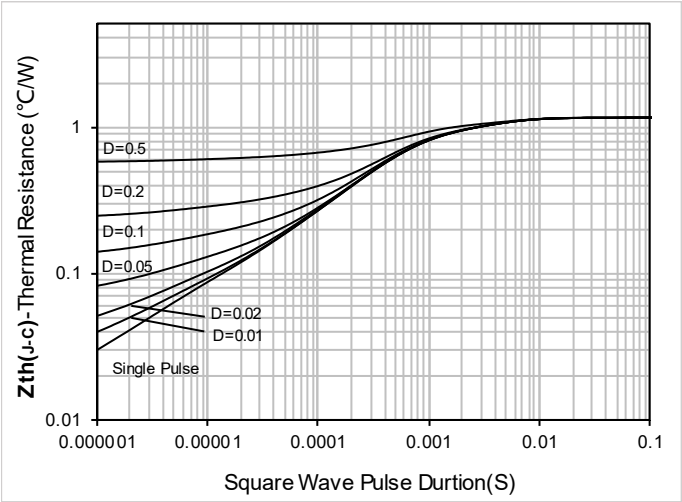


Figure 13. Maximum Transient Thermal Impedance

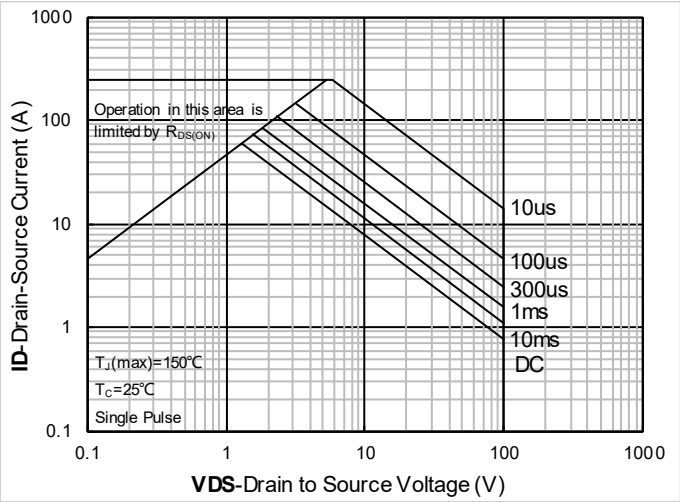


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

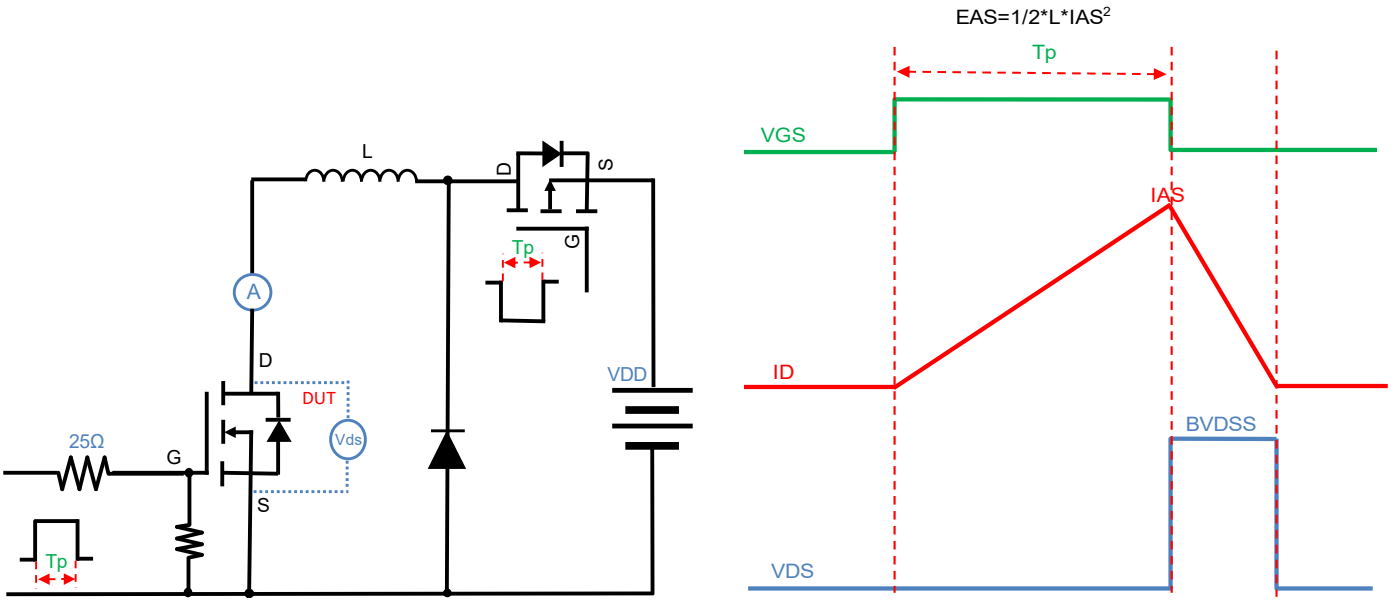


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

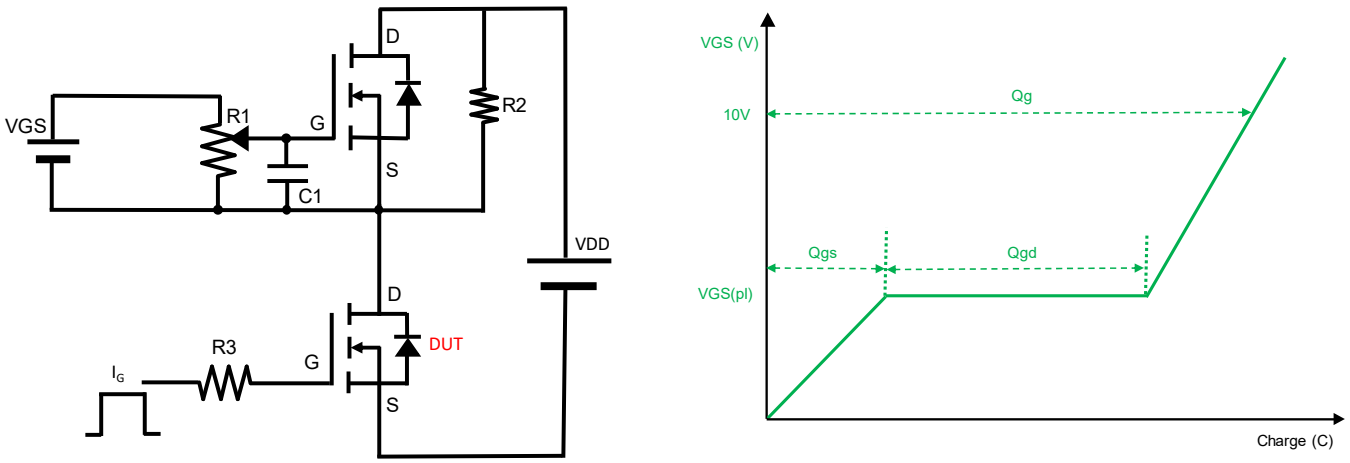


Figure B. Gate Charge Test Circuit & Waveform

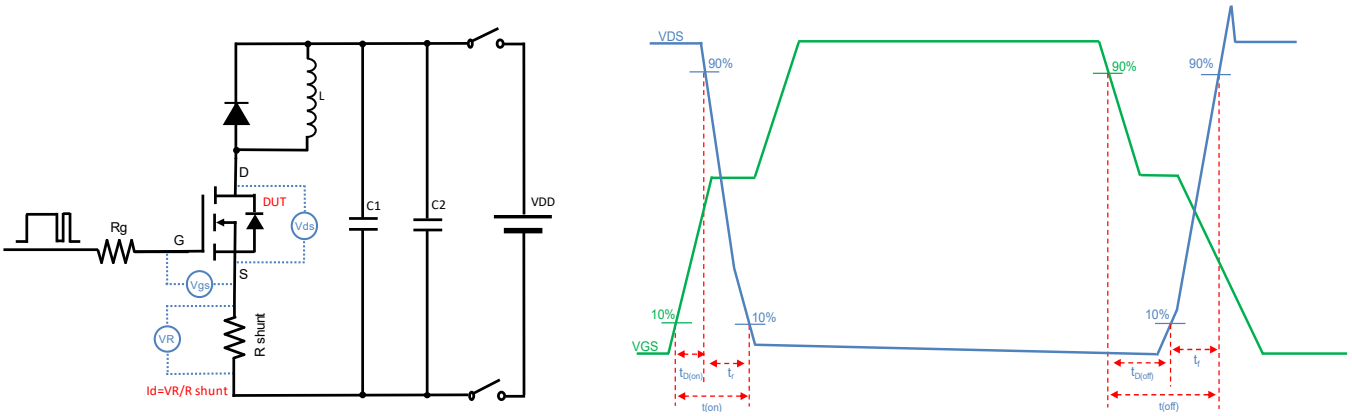


Figure C. Resistive Switching Test Circuit & Waveform

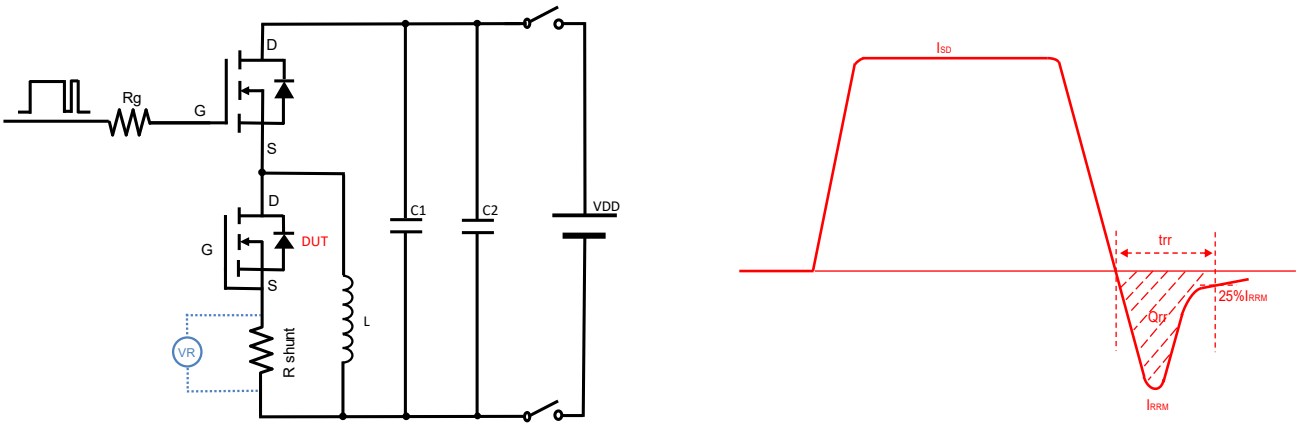
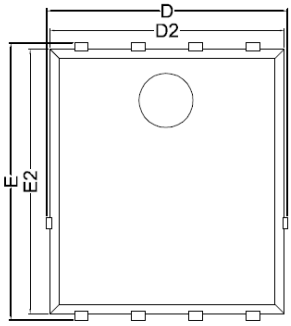
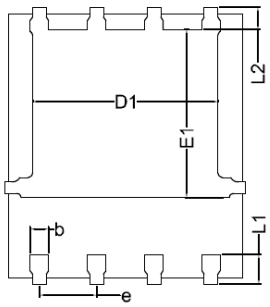


Figure D. Diode Recovery Test Circuit & Waveform

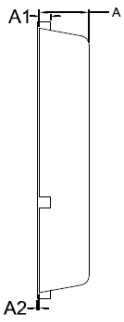
■ PDFN5060 Package information



Top View
正面视图



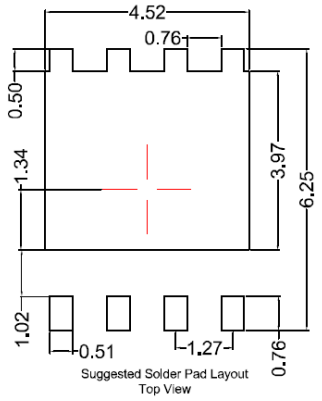
Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
L1	0.56	0.66	0.76
L2		0.50 BSC	
b	0.31	0.41	0.51
e		1.27 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.



Suggested Solder Pad Layout
Top View

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